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# **Metrology and Inspection for 3-D Integrated Circuits and Interconnects**

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Three-dimensional integration of stacked device cells in front end (FE) and of advanced metallization in back end (BE) enabled by through-silicon via (TSV) opens new paths to increased product functionality even without device shrink. But “going 3-D” also creates many new challenges for the semiconductor industry. Development of the new designs, manufacturing methods, and processes demands rapid technology and materials characterization, as well as in-line metrology and inspection for process development and control in completely new and changing applications environments.

This special section in the *Journal of Micro/Nanolithography, MEMS, and MOEMS* (JM3) offers its readers an overview of the key processes, materials, integration, and manufacturing considerations in 3-D IC/3-D interconnect technologies. It also presents a comprehensive account of the state of the art in metrology and inspection, emerging technologies and applications methods, as well as projections as to how these may be practiced in high volume manufacturing (HVM).

The Special Section on Metrology and Inspection for 3-D Integrated Circuits and Interconnects may be the first collection of technology papers in this field. Most papers were contributed by authors who have already published numerous related papers in other journals, presented their work at various conferences and meetings, including SPIE conferences on Metrology, Inspection and Process Control for Microlithography and SEMATECH Workshops on 3D Interconnect Metrology.

The overall structure and technology coverage are as follows:

- Overview
- Metrology for 3-D/TSV Process Development and Control

- Metrology and Inspection for Wafer Bonding Process
- Inspection and Failure Analysis of 3-D Interconnect
- Stress Metrology and Stress Modeling for 3-D Package Design and Process Control

We hope that this anthology will provide a technology introduction for those coming into this field and serve as a useful reference for engineers and researchers using 3-D interconnect metrology in their quest to accelerate the development of TSV based FE and BE product manufacturing technology, advancing metrology and inspection for applications in 3-D IC/3-D Interconnect HVM.

**Alexander Starikov** is an independent consultant DBA I & I Consulting, Palo Alto, California. He received his PhD in physics from the University of Rochester, Rochester, New York ('83). While with Advanced Lithography Systems Development at IBM Corp., East Fishkill, New York, he established rule-based 2-D OPC ('88), certifiably accurate alignment and overlay metrology and performance testing ('88-'94), SEM based overlay metrology ('92). In California since '95, he managed Alignment/Metrology Engineering at Ultratech, leaving for Intel Corp. in '98, where he put into production model-based OPC, pioneered lithography metrology and inspection. He is a SPIE member ('84) and founded Device and Process Integration for Microelectronics Manufacture (2002-3), chaired Metrology, Inspection and Process Control for Microlithography (2011–2013), authored 40+ papers, a book chapter, and seven patents.

**Yi-Sha Ku** is currently a senior principal researcher at ITRI and a professor at National Tsing Hua University. Previously, she worked with National Measurement Laboratory for 11 years and was responsible for the development of primary quantum metrology standards. She has 10 years of experience in the field of overlay metrology and was engaged in model-based method and analysis algorithms, in particular. Her current research interests are developing metrology solutions for three-dimensional interconnect processes.