The Lithography Technology for the 32 nm HP and Beyond

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ABSTRACT

When using the most advanced water-based immersion scanner at the 32nm node half-pitch, the image resolution will be below the k1 limit of 0.25. In this paper, we will explore the capability of using the double pattern technique (DPT) to extend the resolution capability of the water-based immersion lithography and examine the readiness of EUV to carry the lithography resolution capability beyond the 32 nm HP.

The DPT, whether done in two litho and etch steps (LELE) or using the side wall spacer and sacrificial layer technique (SPT), will require significant improvement in CDU and overlay process control performance. We will report the experimental results in exploring the CDU and overlay performance of the LELE and the SPT options. We will also demonstrate the need to perform full field and full wafer process corrections to compensate for dual CDU populations and overlay entangled CDU variations.

Furthermore, we will make an assessment of EUV readiness to further extend the lithography resolution capability beyond the 32 nm half-pitch.

Keywords: double patterning technology (DPT), DPL, LELE, Spacer self-aligned, DPT CDU populations, EUV

1. INTRODUCTION

The resolution limit (at k1=0.25) of the most advanced scanner today is above 35 nm half-pitch. To keep the pace of ITRS device roadmap, extending the ArF water-based immersion lithography becomes necessary because the current state of readiness of the next generation lithography technologies would not be matured in time to satisfy the schedule for the 32nm half-pitch node. The use of double patterning lithography (DPL) has been proposed before [1] to stay on the ITRS roadmap. Now, it has become more prominent because the lack of a single exposure solution available in the desired time frame. [2, 3, 4, 5]

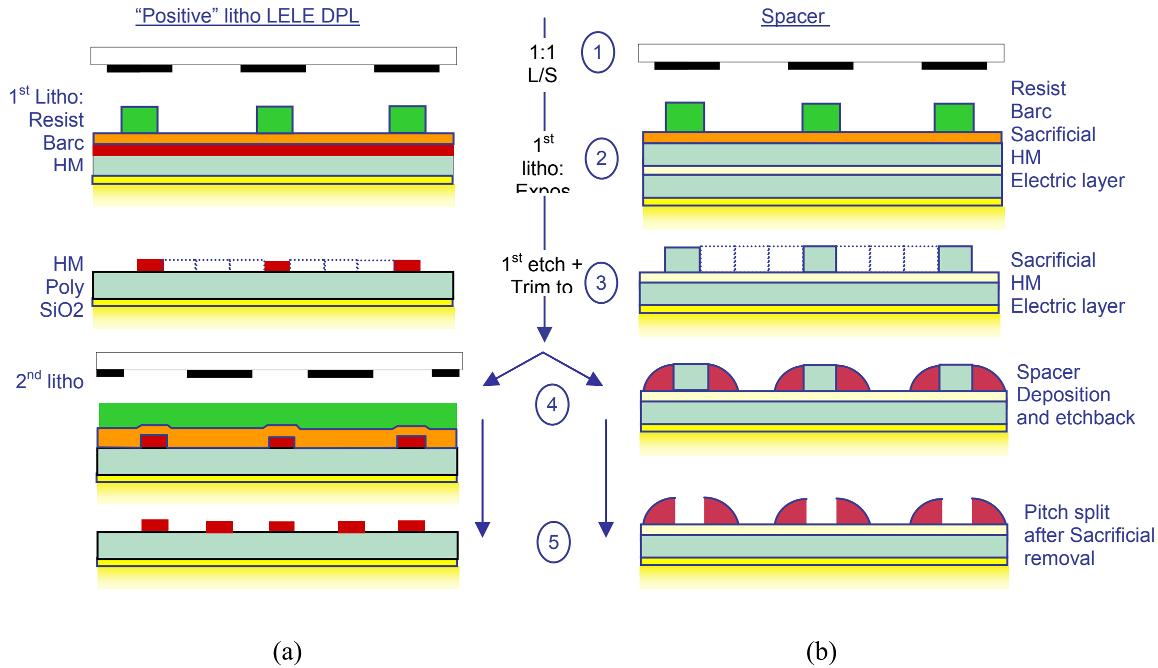
In DPL, each individual litho step takes place at a robust k_1 factor of 0.35 to 0.4, and the subsequent patterning steps, another litho step or other processing to result in a final ½ pitch resolution below k_1=0.25. Compared to the single exposure low k_1 lithography, working at k_1 around 0.40 is favorable for lithographers but it is coming with the added process complexity, significantly lower process tolerance, more metrology and subsequently cost increase. A decision on adopting a lithography double patterning scheme is not anymore determined by litho but by device integration, layout topology, polarity of critical layers and requirements to minimize the impact of dimensional variability on device CDU for either a line or space pattern.

Double patterning schemes have been proposed for Flash and DRAM applications [2,3]. Amongst these, the litho DPL scheme (Litho-Etch-Litho-Etch, LELE) and the self-aligned 'spacer/trim'-DPL scheme (pattern sacrificial layer – sidewall deposition - etch back, then trim) are presented schematically in Figure 1(a) and 1(b).

The LELE scheme, shown in figure 1(a), employs a positive tone resist process. A 1:1 L/S pattern on the mask is exposed to ~1:2 L/S and then etch trimmed down to ~1:3 L/S ratio (steps 1, 2 and 3). This is followed by a 2nd litho and etch (steps 4, and 5). The self-aligned spacer scheme, shown in Figure 1(b), is similar to the LELE during patterning

Photomask and Next-Generation Lithography Mask Technology XV,
edited by Toshiyuki Horiuchi, Proc. of SPIE Vol. 7028, 702810, (2008)
0277-786X/08/$18 · doi: 10.1117/12.796016

steps 1 to 3. Further on, a number of non-patterning process steps replace LELE step 4 and 5, by spacer steps 4 and 5, where a thin, conformal "spacer" layer is being deposited against the sidewalls of a sacrificial hard masks which is removed in step 5.



(a) (b)

Figure 1: Schematic representation of a (a) litho-based and (b) spacer DPL process options.

One of the main distinction of the DPL process shown in Figure 1 is the existence of dual CD distribution of either the lines or spaces of the final pattern formation [6], as illustrated in Figure 2. Next, a detailed CDU error budget of the DPL process and experimental verification data will be provided. A discussion on possible techniques to improve the overall CDU performance will be presented.

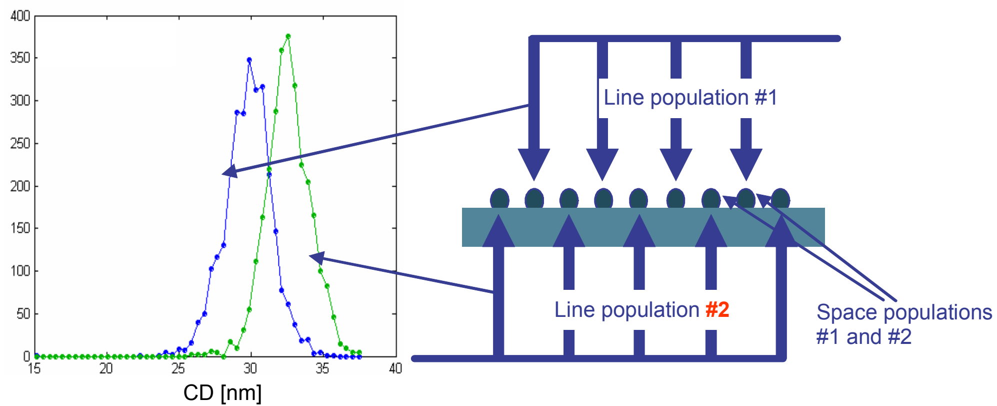


Figure 2. Bi-modal line-CD distribution occurs when CD differs in the two exposures and etch steps. The line populations are different in mean CD and in statistical and spatial distributions. Additionally, overlay error creates a bi-modal CD distribution for space populations.

The use of DPL could be viable down to ~20 nm ½ pitch design rules. As the device further reduces its design ½ pitch, a triple patterning would need to be contemplated. However, it could be a prohibitively expensive process. The

position of EUV is to provide a potential cost reduction to the DPL for the 32 nm to 20 nm ½ pitch processes and an enabling lithography process for below 20 nm design rule products. A brief summary will be given on the EUVL device demonstration activity and possible NA extensions. Then we will conclude on a possible lithography solution path for the 32 nm ½ pitch and beyond.

2. DPL CDU BUDGET AND EXPERIMENTAL VERIFICATION

First attribute of any double patterning scheme is the creation of a single device layer from multiple patterning steps. Second attribute is the direct contribution of overlay, or overlay-type errors, to the CD variation of the final pattern. This is more noticeable in LELE scheme where an overlay error directly modifies the critical dimension of a space or of a line, dependent of the process polarity, positive (= printing lines), or negative (= printing trenches). Although the self-aligned spacer DPL scheme does not use a 2nd patterning step, CD variations during 1st patterning step, can generate a *pitch-walking* occurrence from an induced CD error on spaces between spacer-defined lines that creates an overlay-type of error, comparable to LELE scheme. Third attribute is a consequence of the first two and implies a CDU calculation from pooling two adjacent patterns within 2*pitch distance in order to capture all dimensional errors of a DPL final pattern which consists from two adjacent line-space pairs.

Based on the above attributes, we estimated CDU for two positive tone schemes, Spacer and LELE – see Table 1. We derived the CDU for lines and spaces for a target CD of 32nm L/S, using Monte Carlo simulations [7,8]. For all budget components, we assumed an acceptable level of variations of 10% with variations described by Gaussian distribution and 3σ values. Contributions of track and etch to CD errors was assumed to be 2.4nm (3σ). Furthermore, for LELE, a nominal CD offset of 0.8nm was predicted to be present between averages of line 1 and line 2 CD populations.

With these assumptions, Table 1 shows the presence of two line and two space populations as well as the effect of an overlay error to the space CDU in LELE scheme and of pitch-walking, overlay-like error reflected as the space CD error in the spacer scheme. In the following sections we will describe the experimental work to validate these assumptions as well as the magnitude of contribution and total CDU errors.

Table 1: Predicted CD Populations with contributions from primary components
Estimation for 32nm ½ pitch L/S pattern exposed with 1.35NA

	Positive Tone Spacer		**Positive tone LELE**	
Error component	*Lines*	*Spaces*	*Lines*	*Spaces*
Dose	-	0.7	0.7	0.5
Focus	-	0.5	0.5	0.4
Track and etch process	-	2.4	2.7	1.7
Spacer deposition (+ multiple etch steps)	1.6	2.9	-	-
Mask CDU (1x) (assumes MEEF of 1.4)	-	1.4	1.4	1
Mask registration and overlay (1x)	-	1.1	-	1.5
Scanner overlay	-	-	-	3
CDU - lines (nm)	**1.6**		**3.1**	
CDU - spaces (nm)		**4.2**		**3.9**

Experiments were performed to confirm the adequacy of the proposed CDU budget for DPL. The experimental conditions and equipment used are listed in Table 2.

Table 2: Experimental setup

Exposure	Multiple XT:1900i (ASML VHV) XT:1700i (IMEC)	**Target: 32nm L/S:** annular 1.2 NA XY-pol 0.8/0.5
Reticle	6% Attenuated PSM	64nm L/S
Track	multiple tracks; interfaced to XT:1900 and XT:1700	
Etch	ASML: LELE IMEC: LELE and Spacer	
Metrology	CD-SEM	
Process Control	DoseMapper GridMapper	Intrafield and Interfield dose and grid corrections

For the space CDU control in LELE, the scanner overlay and mask registration are crucial contributors as illustrated in Table 1. The DPL overlay was measured on the final 32nm ½ pitch pattern by CD-SEM using two pitch measurements [7]. The overlay performance verification was done over multiple Twinscan XT:1900i, showed a consistent 3 - 3.5nm single machine overlay (SMO), shown in Figure 3. The scanner overlay performance was consistent to the requirement shown in Table 1 for DPL.

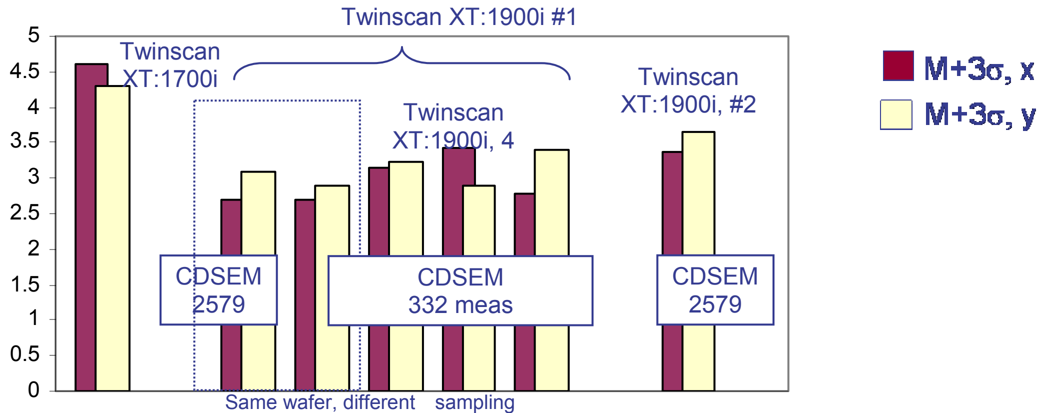


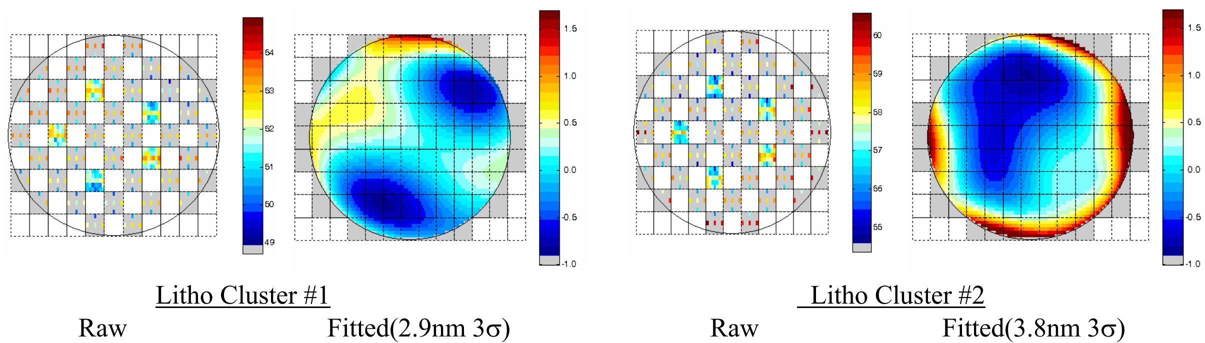
Figure 3: experimental DPL overlay for 32nm ½ pitch by LELE, multiple exposure tools and multiple wafers. Different sampling schemes were used; full: 2579 SEM measurements, reduced sampling for multiple wafers: 332 SEM measurements. For one wafer; the results of the two sampling schemes are compared.

The CDU error contributions from the reticle, track and etcher are shown in Figure 4, 5 and 6 respectively. The reticle contribution to CDU, including the MEEF(1.5) effect, was above the budget allocation. However, this can be compensated partially using DoseMapper. The calculated reticle CD fingerprint after DoseMapper correction was estimated to be 0.4nm , and 0.5nm 3σ respectively. Although the tracks and etchers have different across wafer CDU distributions, the CD fingerprint can also be compensated partially using DoseMapper. The calculated 3σ residual CDU errors after DoseMapper compensation were 1.1nm and 1.4nm respectively for litho cluster #1 and #2, and 1.8nm and

2.0nm respectively for etcher #1 and #2. Thus, DoseMapper is required for the two process line tools used in our experimental study to meet our CDU target of 3.2nm 3σ.

(a) (b)

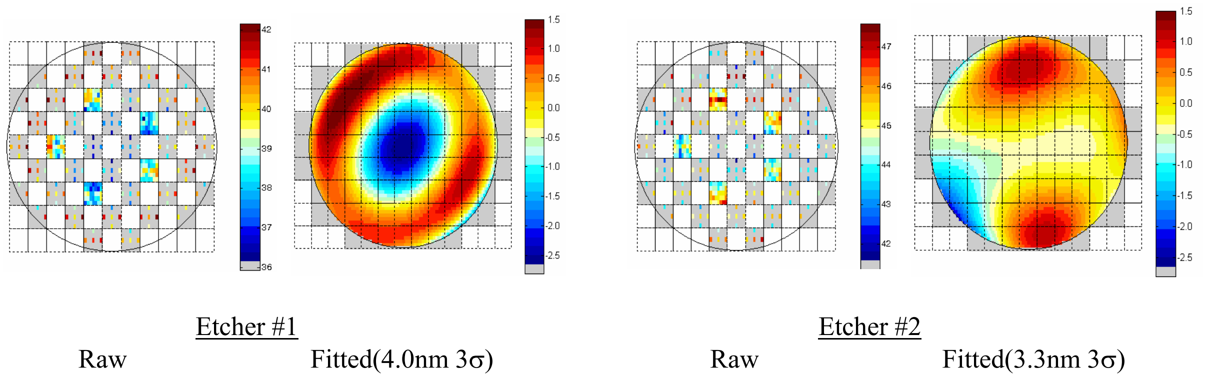
Figure 4: reticle CD fingerprint for three DPL reticle sets, measured with reticle CD SEM (nm CD@1X)
(a) 3σ=0.9nm, and (b) 3σ=0.6nm [9,10] (a) was used for LELE results in this paper. (b) was used to gather experimental results for spacer process.



Litho Cluster #1 — Raw, Fitted(2.9nm 3σ)

Litho Cluster #2 — Raw, Fitted(3.8nm 3σ)

Figure 5: CD fingerprint for two litho-clusters. Raw data as measured by CD-SEM and fitted interfield CD fingerprint are shown. Fit was obtained by applying polynomial fit to the raw CD-data.



Etcher #1 — Raw, Fitted(4.0nm 3σ)

Etcher #2 — Raw, Fitted(3.3nm 3σ)

Figure 6: CD fingerprint after etch of first hard mask in LELE process for two different etch configurations (recipe and hardware).

Knowing the individual contributors to our LELE process, we can start studying the final 32nm ½ pitch pattern. Figure 7 shows the CD fingerprint of the two line populations and the two space populations. The two line populations were offset in mean CD due to different etch biases. Each line population clearly shows the radial etch fingerprint and the intra-die fingerprint coming from the reticle. The space populations were impacted by the overlay performance. The CDU fingerprint from the data shown in Figure 7 was used to calculate the required Dosemapper

corrections. The experimental data after the correction were shown in Figure 8. The lines CDU were meeting the 32 nm ½ pitch requirement as shown in Table1. The spacer control was not as good because of the major contributor was the overlay performance of the scanner and the reticle pattern placement registration errors. Further improvement of the space CDU is expected by improvements in scanner overlay [9].

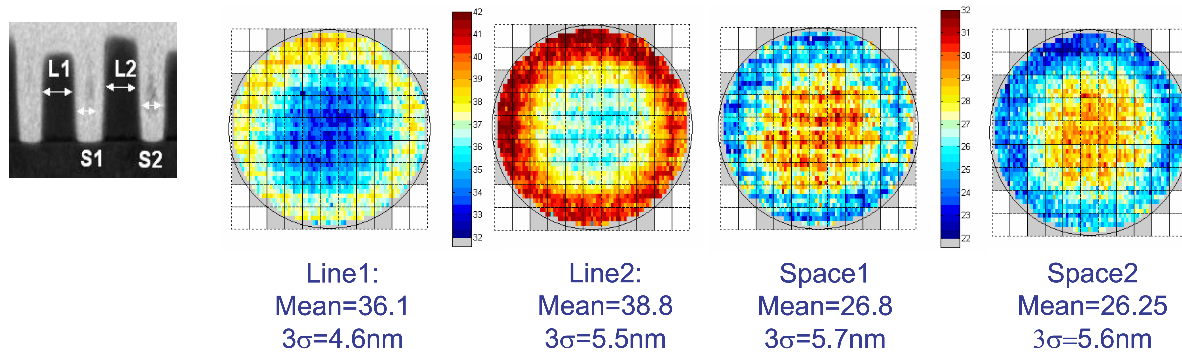


Figure 7: Final experimental CD data for LELE process for 4 features: line 1, line 2, space1, space 2. Exposures on Twinscan XT:1900i, no dose and grid corrections applied.

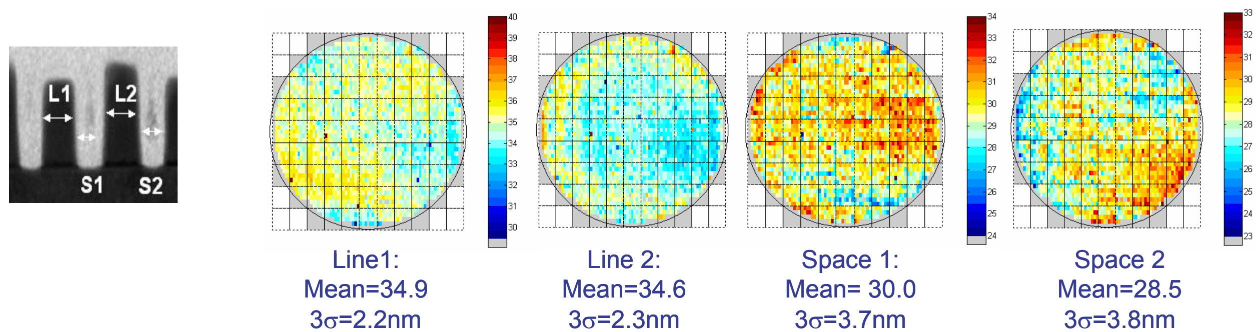


Figure 8: Final experimental CD data for LELE process for 4 features: line 1, line 2, space1, space 2 after applying DoseMapper. Exposures on Twinscan XT:1900i.

The self-aligner spacer scheme has been proposed as an alternative to LELE double patterning because of its superior control of the lines that are patterned by a uniform and conformal deposition of a spacer layer along sidewalls of the sacrificial patterning lines. Furthermore, the formation of the two adjacent lines would not be confounded by the overlay performance. However, effects of litho and etch process deviations from nominal, are predominantly found in CD variation of the sacrificial line which was generated through one litho step and one etch step – see Figure 1(b). According to our estimations shown in Table 1, the CD variations of the sacrificial layer can be caused by variations in scanner's dose and focus, track processing, etch and reticle CDU and registration. On the final doubled patterned layer, these errors are captured as "space" CD variation. Figure 9 shows experimental results from our positive spacer process. The mean and 3σ variations of all four populations are remarkable close to estimated values (from Table 1). As expected, the spacer-defined lines 1 and 2 populations are perfectly correlated in both mean CD and 3σ. Their variation is slightly higher than our 5% prediction, which could indicate about 6.5% non-uniformity of spacer deposition across entire wafer. Variation in space width CD for second space is 4.1nm which is notable close to our estimation of 4.2nm – bear in mind that this variation is from the sacrificial patterned layer.

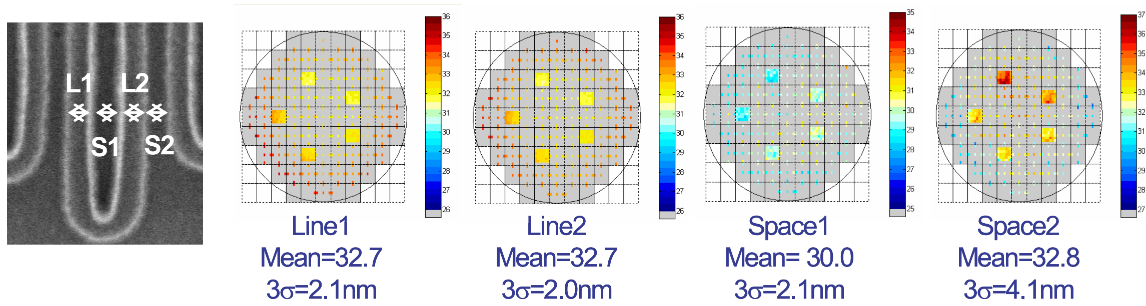


Figure 9. Experimental results from a positive spacer process. Line1 and Line2 are the spacer-defined lines at the left and right edges of the sacrificial pattern. Space 1 is the space width between two spacer-defined lines and Space 2 is the space width defined by the sacrificial patterning and the spacer lines. Exposures on Twinscan XT:1700i.

Again, using the technique of Dosemapper, the mean CD differences between the two space populations can be partially compensated. The expected improvement is summarized in Table 3. The confirmation of the space mean CD control using litho dose adjustment is shown in Figure 10.

Table 3: Four measured CD Populations in spacer scheme
Measured and predicted variations in population mean and variance

		Line 1	Line2	Space 1	Space 2
Before dose corrections (measured)	mean CD (nm)	32.7	32.7	30.0	32.8
	3sigma (nm)	2.1	2.1	2.1	4.1
After dose corrections (expected)	mean CD (nm)	32.7	32.7	31.3	31.4
	3sigma (nm)	2.1	2.1	2.3	2.8

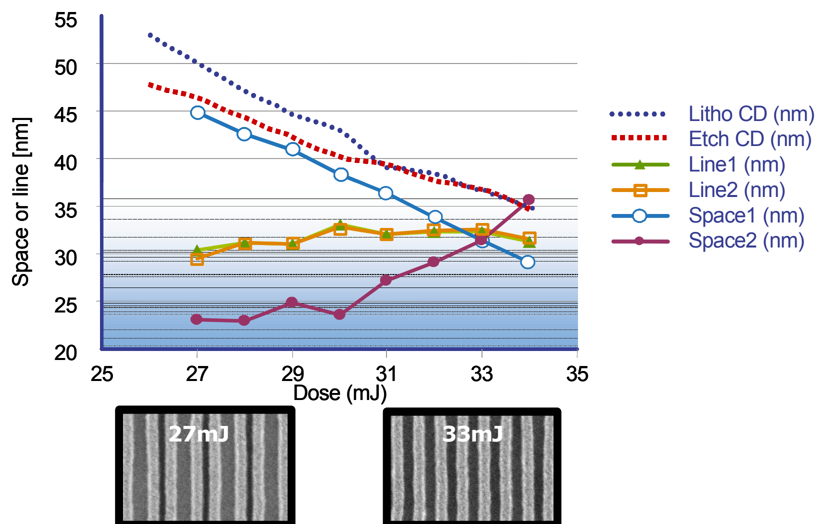
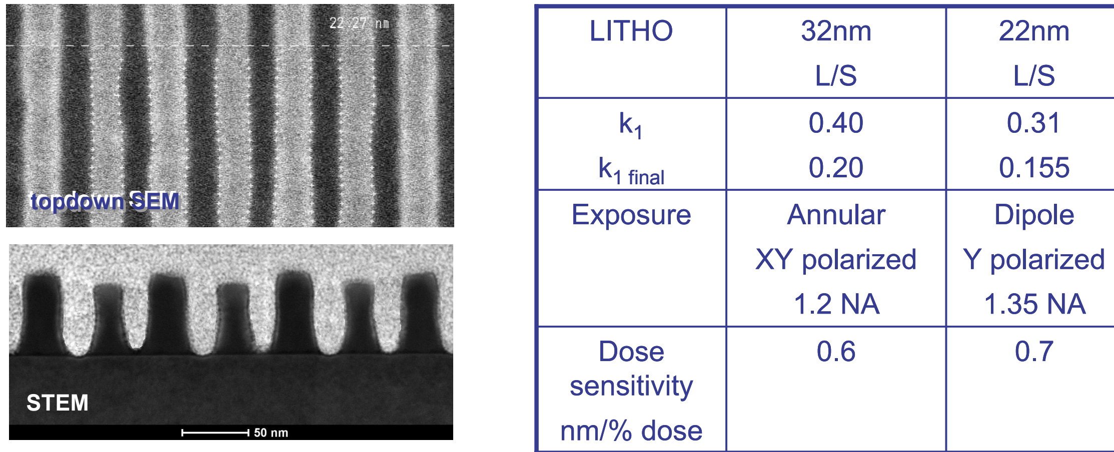


Figure 10. Experimental validation of the control level required to achieve 10% CDU on space width in the self-aligned spacer process. Exposures on Twinscan XT:1900i.

3. CHALLENGES TO GO BEYOND 30NM ½ PITCH

Significant challenges exist to extend the DPL to the 20nm ½ pitch region. In the lithography area, one can adopt a more aggressive illumination such as dipole to maintain the image contrast similar to the condition shown for the 32 nm ½ pitch example. An early experimental result performed at 22nm ½ pitch is shown in Figure 11. As we have illustrated previously of the complex processing involved in any of the DPL techniques, one of the major challenges is to provide the needed process control to maintain the CDU and overlay performance.



LITHO	32nm L/S	22nm L/S
k_1 $k_{1\ final}$	0.40 0.20	0.31 0.155
Exposure	Annular XY polarized 1.2 NA	Dipole Y polarized 1.35 NA
Dose sensitivity nm/% dose	0.6	0.7

Figure 11. Experiment result of a LELE patterning of 22nm ½ pitch line/space structure.Exposures on Twinscan XT:1900i.

The other alternative is the use of EUV. EUV has the advantage of a single exposure solution to extend the lithography resolution capability in the 1xnm ½ pitch region. There are two full field research exposure scanners [10], at 0.25NA, to conduct active development activities for the semiconductor industry. Recently a SRAM layer was processed successfully using EUV [11]. One of the ASML exposure systems was used to evaluate the first lithography processing for 32nm-node SRAM structures. Figure 12 shows the resist image simulation result of the targeted SRAM cell and also a first exploration of the exposure latitude for a dose range between 13.5 and 15.5 mJ/cm^2. More work is in progress to complete the SRAM cell, and details of this work can be found in [12].

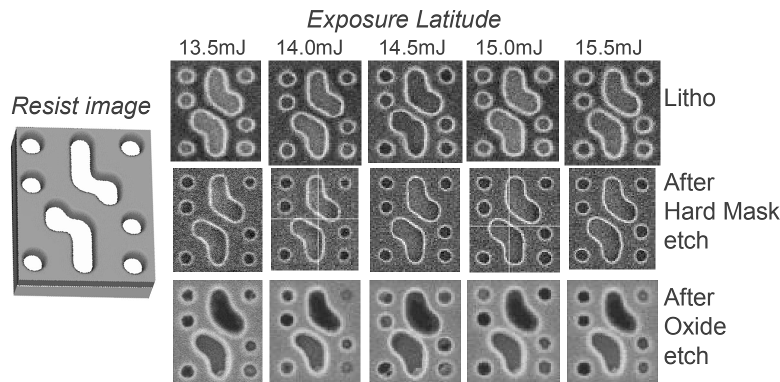


Figure 12. Resist image simulation and exposure latitude evaluation of SRAM cell – in resist, after hardmask etch, and after oxide etch, from [12] and [10].

Furthermore, NA higher than 0.25 is being investigated [13]. An example of higher NA EUV lens designs are shown in Figure 13. This allows the extension down to the 1xnm ½ pitch at relative high k1 factor. The challenges of EUVL remain to be in the infrastructure. However, consistent improvement has been demonstrated in all areas; such as the EUV source power [14], reticle blank defect improvement - now down to 0.04 defect/cm^2 [15], resist capability [16] and resist contrast loss reduction [17]. For example, the diffusion length of chemical amplified resists can degrade the high EUV aerial image contrast as shown in Figure 14(a). Recent resist development has shown an improvement in reducing the diffusion effect, as shown in Figure 14(b), that the resist type B can maintain the exposure latitude as the half-pitch decreased [17].

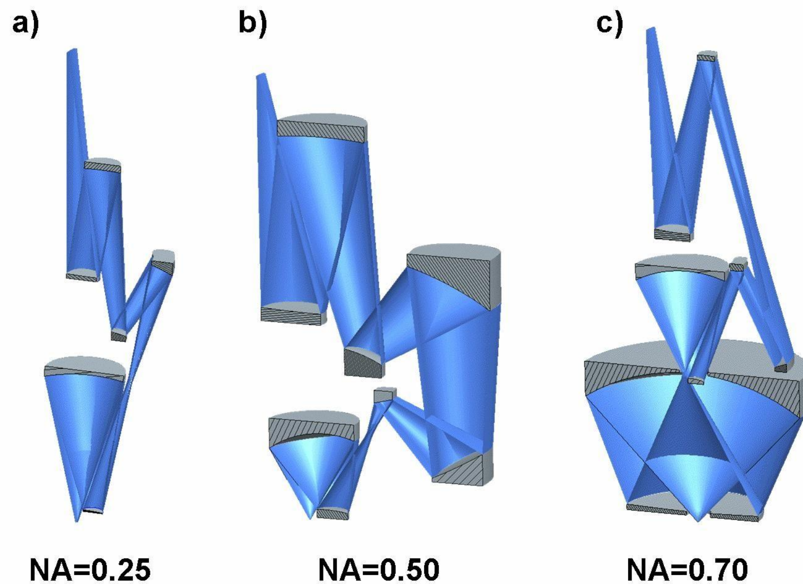
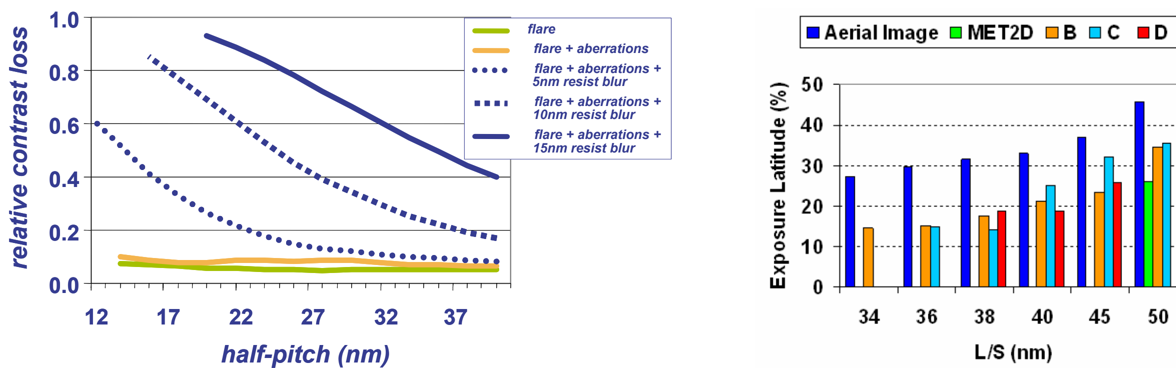


Figure 13*[*] Example of higher NA EUV lens designs. (a) 6 mirror design for 0.25 NA, (b) 0.5NA using an 8 mirror design, (c) extension of 8 mirror design to 0.7NA, with a central obscuration



(a) (b)

Figure 14 (a) simulations results of the relative contribution of EUVL error sources, showing the significant image contrast loss due to resist diffusion effects. (b) experimental data showing the improvement of resist contrasts, from [17].

* With permission from Carl Zeiss SMT AG.

4. CONCLUSIONS

Due to the capability to shrink the pitch below 0.25k1, DPL is a natural resolution extension for ArF immersion lithography. Compared to single exposure lithography, DPL resolution benefits are coming with trade offs from added process complexity, significantly tighter CDU and overlay control and increased metrology. In this paper we reported results of hyper-NA litho system integrated with etch and other processing tools to explore CDU and overlay performance at 32nm ½ pitch resolution in LELE and self-aligned spacer DPL schemes. A key challenge is the control of the multiple CDU populations created during independent patterning steps. For LELE scheme, we identified four independent CDU populations, two for lines and two for spaces. Line CDU populations, generated from the two independent Litho and Etch steps, have different averages with different statistical and spatial distributions. Mean difference between two space CDU populations are correlated to the overlay error between layer1-to-layer2, while their spatial and statistical distribution could be different. In the self-aligned spacer scheme, we recognized also four populations, three of them being clearly separated in their averages and distributions. In a positive spacer process, the two line CDU populations are perfectly correlated with almost equal means and 3σ distributions. The two associated space CDU populations have different means and distributions. Dimensional imbalance of the two space CDU populations behaves like a local overlay error.

The biggest DPL challenge is to control the whole process as an integrated system. Sources of CDU error from all components of the patterning system become visible: reticle CDU & registration, wafer spatial distributions caused by film deposition (stress), etch fingerprint, PEB, and metrology. This interconnectedness coupled with sub-half nm control tolerances motivates application of active compensation control of both CDU and overlay. By applying the active compensation technique, we reported CDU control levels of 2nm and overlay control of ~3nm, which support future adoption of double patterning as the resolution enhancement solution at 32nm node.

There is a significant process control challenge to further extend DPL down to the 2xnm ½ pitch region. EUV can become a viable alternative for the 2x and even down to 1xnm ½ pitch using a higher than 0.25NA aperture. The success of EUVL will depend on the infrastructure maturity. An example of the resist development has shown significant progress are been made.

ACKNOWLEDGEMENT
We would like to acknowledge entire DPL teams at ASML and IMEC, and EUV teams at ASML, IMEC and Albany for their support and outstanding work results.

REFERENCES

1. A. Ebihara et al. , *Beyond k1=0.25 lithography : 70nm L/S patterning using KrF scanners*, Proceedings of SPIE 5256, 2003
2. Woo-Yung Jung, et al, *Patterning with amorphous carbon spacer for expanding the resolution limit of current lithography tool,* Proceedings of SPIE 6156-27, 2006
3. Chang-Moon Lim et al, *Positive and negative tone double patterning lithography for 50nm flash memory,* Proceedings of SPIE, Vol.6154-37,2006
4. S-M Kim et al, *Issues and challenges of double patterning lithography in DRAM*, Proceedings of SPIE, Vol.6520-17, 2007
5. M. Maenhoudt et al, *Double patterning scheme for sub-0.25k1 single damascene structures with NA=0.75, λ=193,* Proceedings of SPIE Vol. 5754, 2005
6. J. Finders et al, *Double patterning for 32 nm and below, an update*, Proceedings of SPIE, Vol. 6924, 2008
7. M. Dusa et al, *Pitch doubling through dual-patterning lithography challenges in integration and litho budgets; Pitch doubling through dual-patterning lithography challenges in integration and litho budgets,* Proceedings of SPIE Vol. 6520, 2007
8. J. Finders et al, *Double Patterning Lithography: the Bridge Between low k_1 ArF and EUV*, MLW, March 2008
9. J. de Klerk at al, *Latest developments on immersion exposure systems*, Proceedings of SPIE, Vol. 6924, 2008
10. H. Meiling et al, Performance of the full field EUV system, Proceedings of SPIE, Vol. 6921, 2008
11. B.M. LaFontaine et al, *Use of EUV lithography to produce demonstration devices*, Proceedings of SPIE, Vol. 6921, 2008.
12. G. Lorusso et al, *Imaging performance of the EUV alpha demo tool at IMEC,* Proceedings of SPIE, Vol. 6921, 2008
13. W. Kaiser et al, *The future of EUVL*, Proceedings of SPIE, Vol. 6924, 2008.
14. D.C. Brandt et al, *Laser-produced plasma source system development*, Proceedings of SPIE, Vol. 6921.
15. International Sematech press release, Feb 11, 2008.
16. T. Wallow et al, *Evaluation of EUV resist materials for use at the 32-nm half-pitch node*, Proceedings of SPIE, Vol 6921, 2008
17. Koen van Ingen Schenau et al, *Photoresist induced contrast loss and its implication on EUV imaging extendibility*, Proceedings of SPIE, Vol. 6923, 2008.