MEMS above IC technology applied to a compact RF module

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ABSTRACT

Miniaturization, low cost and excellent performances at microwave and millimeterwave applications represent the main leitmotivs of the future mass market communication systems. Consequently, a novel "MEMS above IC" technology has developed in order to allow the elaboration of post-processed micro-machined passive components on top of SiGe circuits to realize a complete short-range communication receiver centered at 24 GHz.
The developed technology is based on the use of :

- ✓ a thick organic layer (BCB), which is employed as a dielectric membrane,
- ✓ metallizations to realize the passive metal layer and also the vias to interconnect the active circuits with the post-processed passive components,
- ✓ and a bulk silicon micromachining.

This 'above IC' technology presents many advantages, as it uses conventional equipments of microelectronics and is in adequation with high frequency applications. A specific attention has been carried out in order to assure the compatibility of the post-process steps and the IC's. This has been performed through the choice of the adequate technological steps, which had to present a low temperature budget. The compatibility of each step has been evaluated with a specific test protocol on SiGe transistors. It implies static and dynamic characterisation of these transistors as well as low frequency noise measurements. Each step has been validated, even the bulk silicon micromachining. Design rules have thus been defined in order to localize the silicon etching without any damage on the ICs.

Keywords : polymer, microwave, millimeterwave, silicon, micromachining, MMIC, process compatibility

INTRODUCTION

In order to fulfil the miniaturization requirement of the future communication systems at low cost and with excellent performances, new technological solutions are investigated to reach even higher frequencies. In literature, some of these technologies are based on the use of silicon micromachining [1-2] in order to realize suspended components, whereas others employs polymers to elaborate low losses circuits [3-6] on top of MMICs.

This paper proposes a technological solution founded on the post-processing of suspended antenna on top of SiGe circuits at 24GHz. The basic schematics of such structures are presented in Figure 1.

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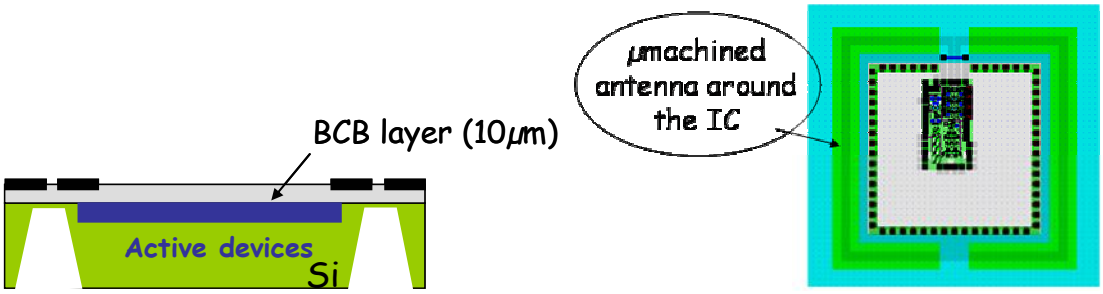


a) b)

Figure 1. Schematics of an antenna with micromachined trenches: a) cross section and b) top view

In order to reach low loss level and to minimize the radiation of the antenna, a micromachined configuration has been chosen on top of active SiGe devices. The antenna is localized all around the IC. The localization of the IC has been specifically studied in order not to deteriorate the antenna performances [7].

First part of this paper will describe the developed technological process flow. This will imply the determination fo the limit temperature that the SiGe circuits may handle without any degradation. The dielectric membrane choice as well as the silicon etching technique will then be explained.

The second part will be dedicated to the compatibility study of the post-process with the SiGe components. And the third part will deals with the final demonstrators description and elaboration.

1. TECHNOLOGICAL PROCESS FLOW

1.1. Determination of the limit post-process temperature of SiGe circuits

In order to assure the performances of the IC's at the end of the post-processing, their limit temperature has been studied. It has been performed by applying a temperature ramp on a SiGe wafer with test transistors and checking their static and low frequency noise performances. These tests translate indeed any internal modification of the transistor at the heterostructure level.
Because of the long time required for the low frequency noise measurements, only four different temperatures have been tested: 300, 330, 360 and 400°C.

Figure 2 presents the low frequency noise measurements of one test transistor. It has been realized with a V_{CE} of 2V, a V_{BC} of 0V, a base current of 20µA and a collector current of 4.72mA.

Important changes are noticeable above 330°C. Generation-recombination centers are present on the red (360°C) and blue (400°C) curves and a frequency shift is obtained to higher values with an increase of the temperature stress.

Changes above 330°C have also been obtained on the static performances, as shown in Figure 3. Black and pink curves, which are related to the 300°C and 330°C respectively, are very close to each other, whereas a big gap between 330°C and 360°C in red is visible.
As well as for the noise measurement, a similar modification of the transistor behavior is achieved for temperature higher than 330°C.

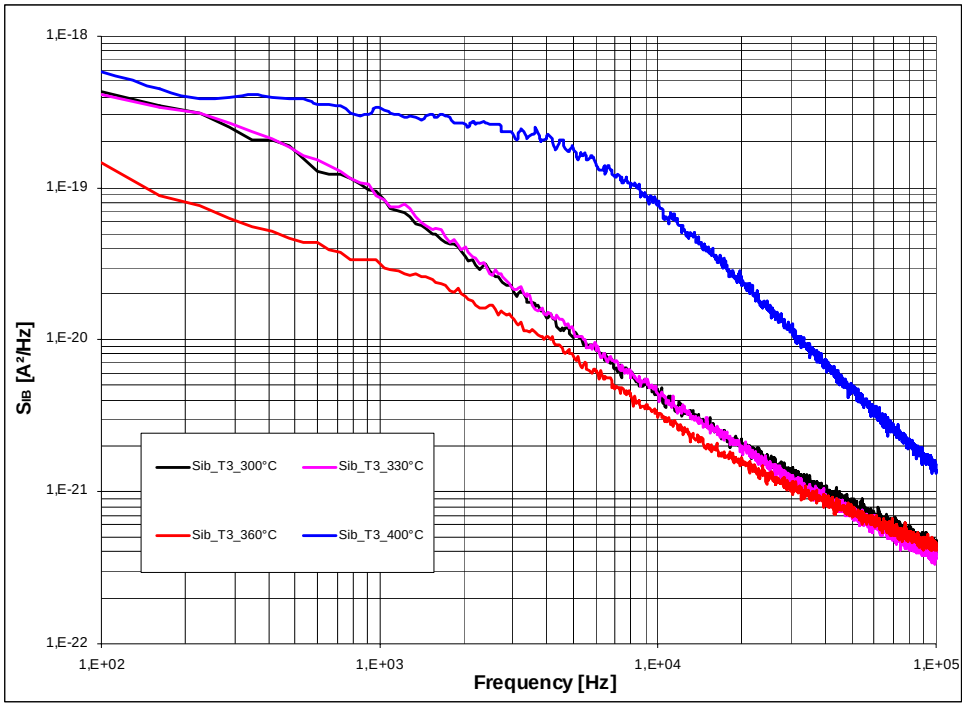


Figure 2. Low frequency noise spectrum density on the base current during a ramp temperature

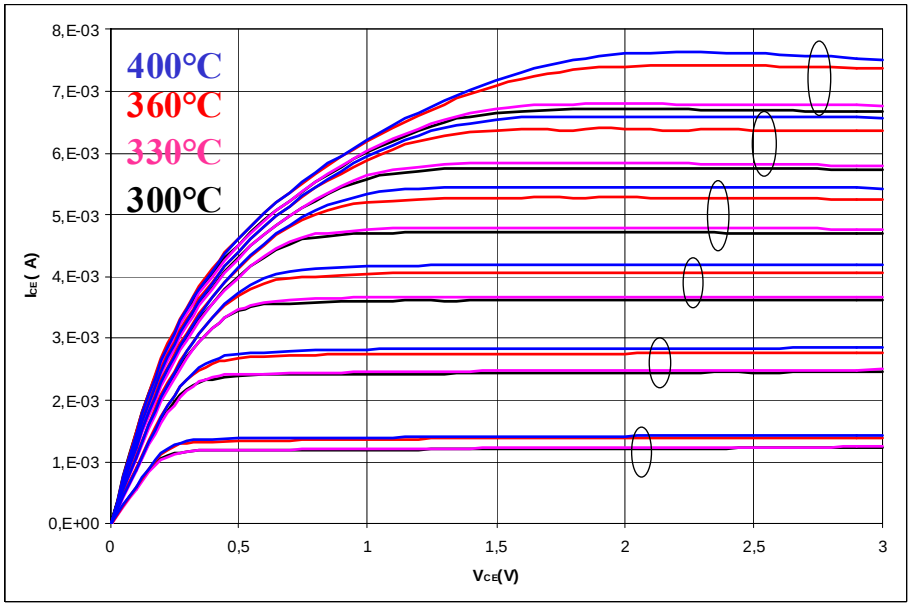


Figure 3. Static performances of a test transistor during a temperature ramp

In conclusion, the limit temperature handled by the SiGe transistors without any important deterioration is situated between 330°C and 360°C. In order to avoid any trouble, only temperatures below 330°C should be employed for post-processing.

1.2. Choice of the dielectric membrane

As far as the dielectric membrane is concerned, three different types exist:

- ✓ mineral membrane, based on the use of thermal silicon oxide and nitride layers. However, their process temperatures are close to 1000°C, which are really unacceptable for circuits realized with SiGe heterostructures.
- ✓ Still mineral membrane (SiO_2 and SiN), but realized through Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. The corresponding temperature is below 330°C, but the global stress remains quite high with values close to 600MPa. To realize robust membrane without any problem of buckling, the global stress of the different dielectric has to be kept below 50MPa and in tension. To fulfil this requirement, an annealing with a temperature of 700°C has to be performed to reduce the stress. Here again, the temperature is not acceptable with SiGe IC's.
- ✓ Finally, polymer membranes only require cure temperature below 330°C. Benzocyclobuten (BCB) from Dow Chemicals has been chosen as dielectric membrane, as it presents low loss tangent even at high frequencies [8]. Vibration and shocks tests have been performed on such membrane and no failure mechanism have been encountered.

1.3. Choice of the silicon etching technique

The two possible silicon etching techniques are shown in Figure 4. One is humid with the use of a KOH bath, whereas the other one is dry (Deep Reactive Ion Etching, DRIE).

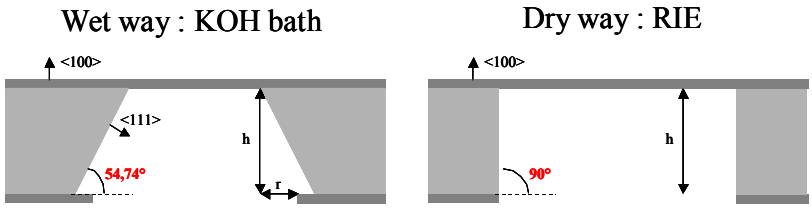


Figure 4. Schematics of the two silicon etching types : a) wet and b) dry

❖ **KOH etching**

The wet etching of the silicon substrate is realized in a KOH bath at 80 °C. The etching time depends on the substrate thickness and corresponds approximately to 4 hours for a 400µm thick wafer.

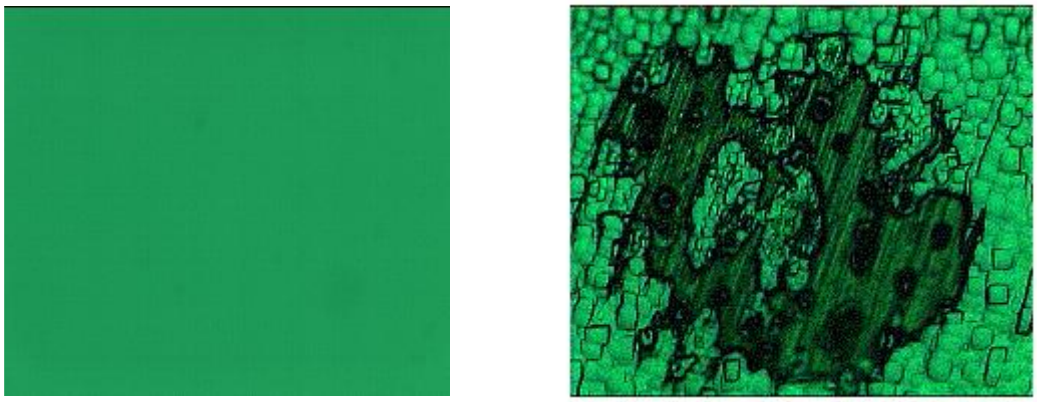
This anisotropic etching method is well-known for its main drawback: contamination. In order to avoid this problem and protect the front-side of the wafer with the active devices, the wafer is sticked with a special wax on a glass substrate.

❖ **Deep Reactive Ion Etching (DRIE)**

The DRIE consists in applying a plasma on the substrate, which attacks the silicon atoms. The thickness of the substrate determines, as well as for the KOH technique, the etching time. A thick photoresist mask is used in this process. It is deposited and patterned on the back-side of the wafer. In order to minimize the stress applied to the wafer during the DRIE process, the wafer is bonded to another one, which is metallized on the back-side. Both the metallization and the bonding wax permit to better evacuate the temperature increase during the process step. This technique permits to get straight etching angles, which allows a stronger compactness of the passive components, compared to the humid micromachining.

On the other side, a silicon nitride mask is required in the case of the humid technique. This layer is obtained by PECVD in order to minimize the deposition temperature to reasonable values acceptable by the IC's (below 300°C).

This mask has been used both on a standard silicon wafer and on a SiGe substrate from ATMEL. Figure 5 indicates the pictures of this SiN layer after few minutes spent into a KOH bath for both substrates.



a) b)

Figure 5. PECVD silicon nitride on a). standard silicon wafer and b) SiGe wafer

This experiment indicates that the SiN layer is deteriorated with the etching bath only in the case of the SiGe wafer. The adhesion and composition of the nitride layer is totally different for both substrates. This is due to the roughness of the SiGe wafer, created during the polishing and thinning step of the wafer.
Consequently, the DRIE technique has finally been chosen.

1.4. The complete technological process flow

The micromachined "above IC" technology is presented in Figure 6. This technological process is divided in six main steps.

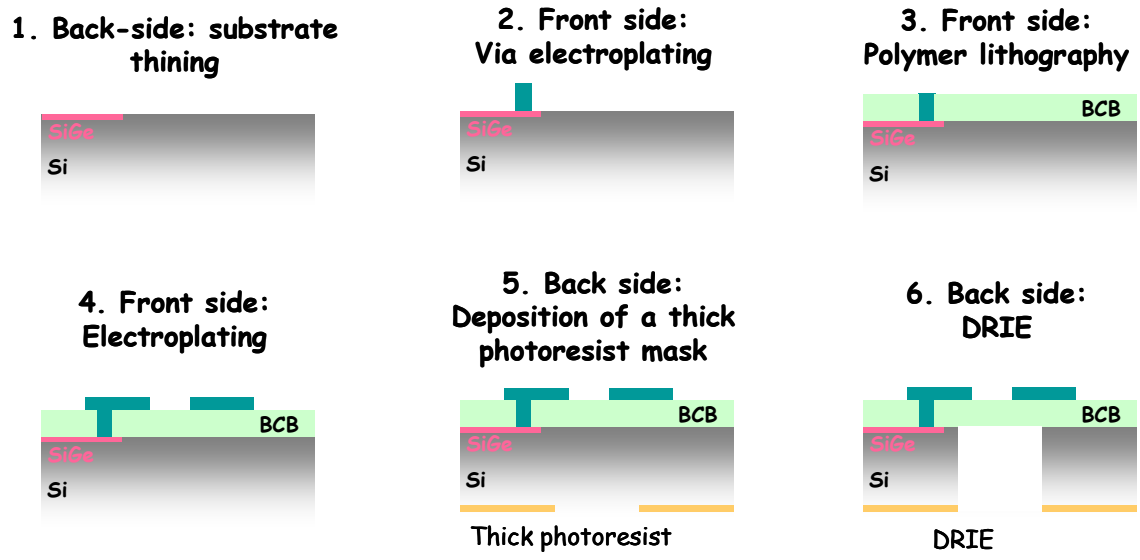


Figure 6. Micromachined above IC technological process flow

First, the SiGe wafers are thinned by the founder ATMEL from 650µm to 400µm in order to minimize the final silicon etching time. After a cleaning step and a plasma treatment (step 1), a Ti/Au seed layer is evaporated and

followed by the electroplating of 10µm thick gold vias into a photoresist mould (step 2). These vias are used to to interconnect the IC's with the post-processed antenna. This photoresist mould is then removed. A plasma treatment is performed just before the patterning of the polymer layer (step 3) in order to favour the adhesion of the BCB. The polymer is then deposited and patterned, with the elaboration of openings on top of the vias. A hardcure at 250°C during one hour under a nitrogen flow is then performed to polymerize the BCB layer. Next step corresponds to the gold electroplating of the antenna on top of the vias. Once again, a seed Ti/Au layer is evaporated. The antennas metallization is then obtained with a gold electroplating into a thick photoresist mould. After the suppression of the mould, the seed layer is suppressed in the slots. This is followed by the Si DRIE (Deep Reactive Ion Etching) through a thick photoresist mould. For this last step, the wafer is sticked on a support one with a photoresist in order to avoid the breaking of the membranes. Finally, the structures are released from the support substrate with an acetone bath.

As a first validation of the post-process, antennas without "SiGe substrate" have been realized and characterized. An example of such antennas with trenches is presented in Figure 7. Top and back side pictures are shown.

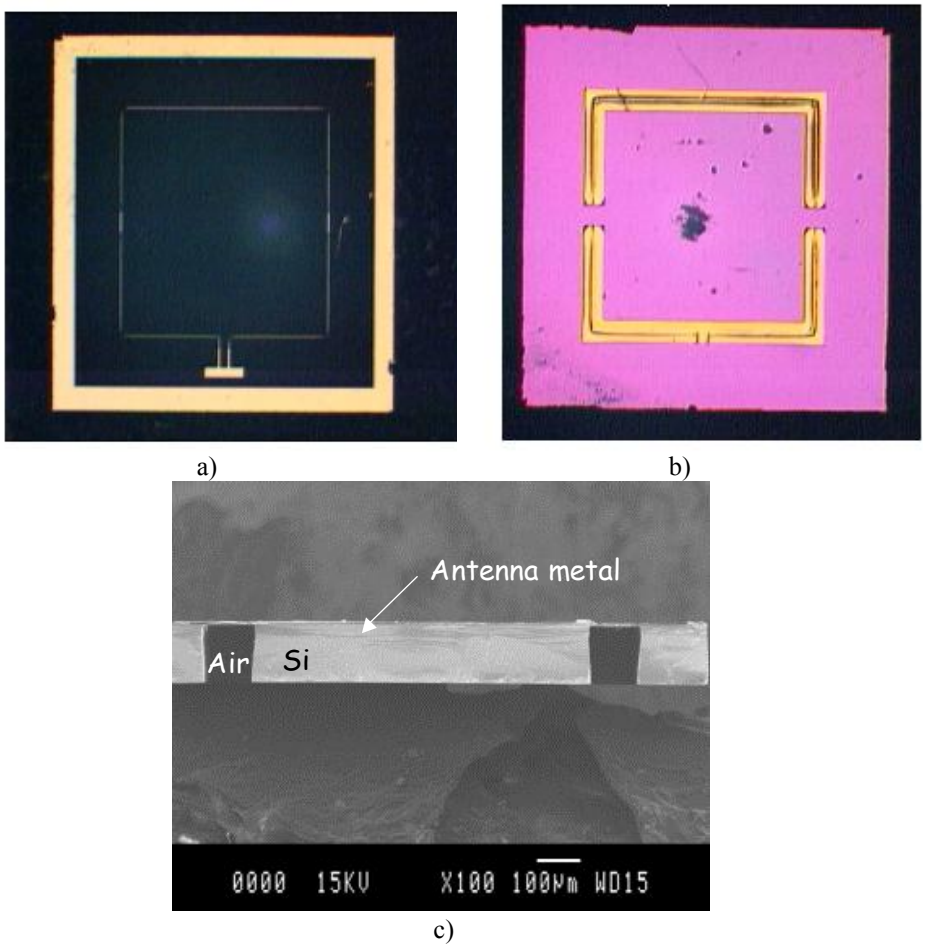


Figure 7. Pictures of an antenna with trenches seen from: a) the front side, b) the back side and c) the SEM cross section

In Figure 7.b, the BCB membrane transparency permits to recognize the slots in the metallization. The trenches are well-defined in the cross view shown in Figure 7.c. They present straight angle without any damage of the membrane.

In order to employ this technology with SiGe circuits, its compatibility with the IC's has been investigated.

2. POST-PROCESS COMPATIBILITY WITH IC'S

This part presents the study of the post-process compatibility with IC's. SiGe wafers from ATMEL have been used to realize this investigation. The most important and critical technological steps in term of temperature, contamination and charges have been tested with a specific protocol indicated below.
These steps correspond to the following ones:

- Polymer deposition and patterning
- Oxygen plasma treatment
- Bulk silicon micromachining.

2.1. Standard test protocol

In order to define the impact of the critical technological steps on the SiGe circuits, a test protocol has been used. It is divided in three steps:

- Pre-measurements of test transistors are performed: static and low frequency noise measurements.
- The technological stress is then applied on the test wafer.
- Post-measurements of the same transistors are realized and then compared to the pre-measurements.

The frequency range starts from 100 Hz to 100 kHz in the case of the low frequency noise measurements. The results of the pre-measurements are used then as reference in order to evaluate the impact of each technological stress.

2.2. Polymer deposition and patterning

BCB membranes (benzocyclobutene from the Dow Chemical Company) have been chosen because of their attractive properties. Concerning its technological step, it starts with the deposition of an adhesion promoter called AP 3000 on top of the silicon substrate. The BCB layer is then spun on the wafer. After drying the organic layer at 90 °C for 60 seconds, we proceed, if needed, to a patterning of the photosensitive BCB. A polymerization follows at 250 °C for 60 minutes in a nitrogen atmosphere.

Figure 8 presents the low frequency noise measurements of a test transistor. This measurement has been realized with a V_{CE} of 2V, a V_{BC} of 0V, a base current of 8µA and a collector current of 1,26mA.

No real modification of the spectrum is noticeable with the process stress. The small difference between the two curves may be induced by the measurement set up, especially the probes position. No change has also been detected for both static performances and Gummel plot.

These results demonstrate that the BCB process, including the BCB deposition, its patterning with its corresponding chemicals and the hardcure at 250°C for the polymerization, has no influence on the test transistors characteristics. No problem of contamination and deterioration induced by the chemicals and the annealing temperature were encountered.

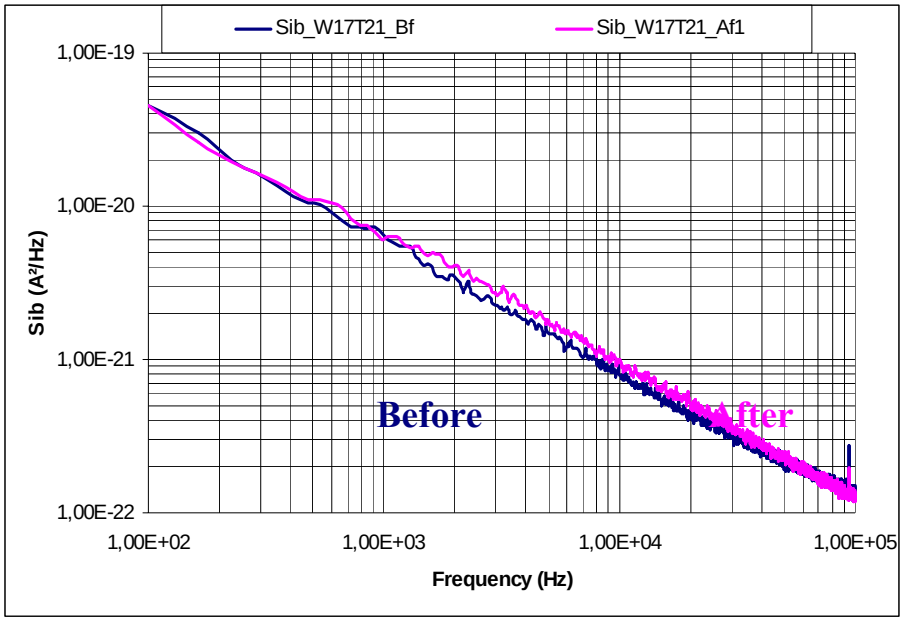


Figure 8. Low frequency noise spectrum density on the base current before and after BCB process

2.3. Oxygen plasma treatment

Before the elaboration of the conductors, an oxygen plasma treatment is performed on the BCB layer. This step permits to improve the adhesion of Ti/Au seed layer evaporated on the polymer layer, as it increases the roughness of the BCB surface. A light oxygen plasma is realized for 2 min at 200 Watts. During this step, the temperature does not exceed 34 °C. However, the use of a plasma could be a source of internal modification of the transistors, especially charges and generation-recombination traps.

In order to study the impact of the plasma treatment on the characteristics of active devices, we have proceeded to the same measurement protocol.
As well as for the BCB process, no modification of the test transistors performances was encounterd during the static and low frequency noise evaluations.
Consequently, the oxygen plasma treatment does not deteriorate the performances of the active devices.

2.4. Silicon micromachining impact

Bulk silicon micromachining is used in the elaboration of dielectric membranes, which minimize losses and dispersion induced by the silicon substrate. The impact of this crucial process step has also been evaluated in term of compatibility with SiGe transistors.
Figure 9 indicates the low frequency noise measurement obtained before and after Si etching through DRIE.

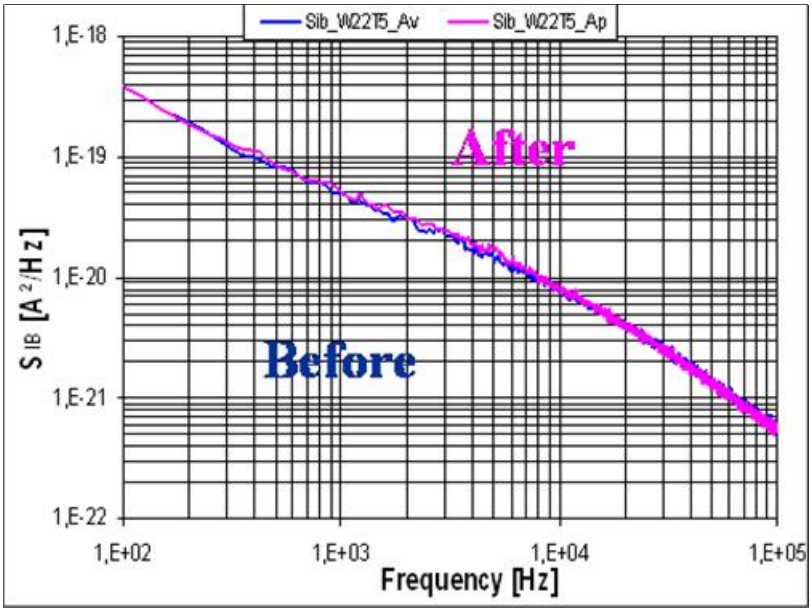


Figure 9. Low frequency noise spectrum density on the base current before and after BCB process

No static and noise measurements deterioration has been obtained at specific localization of the silicon micromachining. This important result permits t

To conclude this part, critical technological steps of the post-process have been evaluated and validated in term of compatibility with SiGe IC's.

3. FINAL DEMONSTRATORS

Thanks to the compatibility study, the post-processed has then be applied to the final demonstrators. Two examples of structures are presented in Figure 10. In green corresponds the localization of the future membrane with the antennas on top.

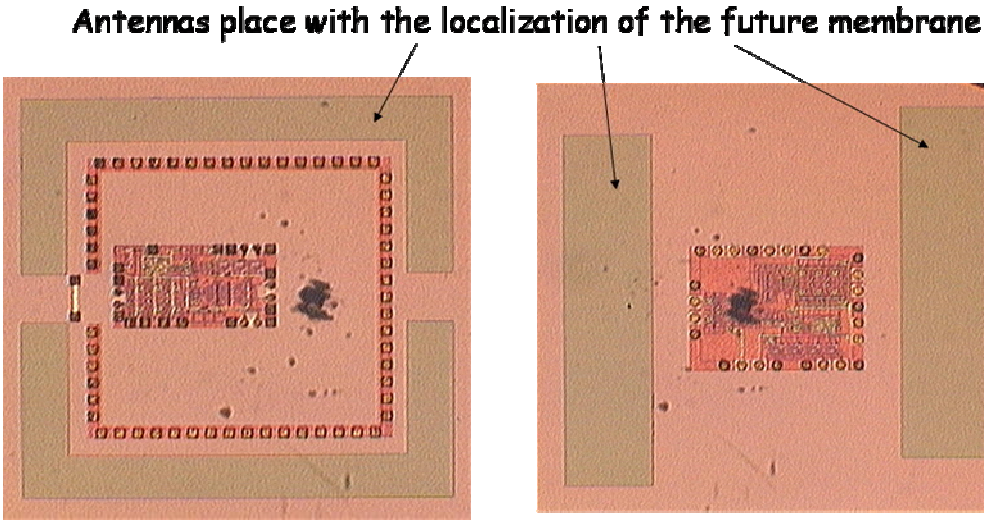


Figure 10. Examples of structures before post-processing

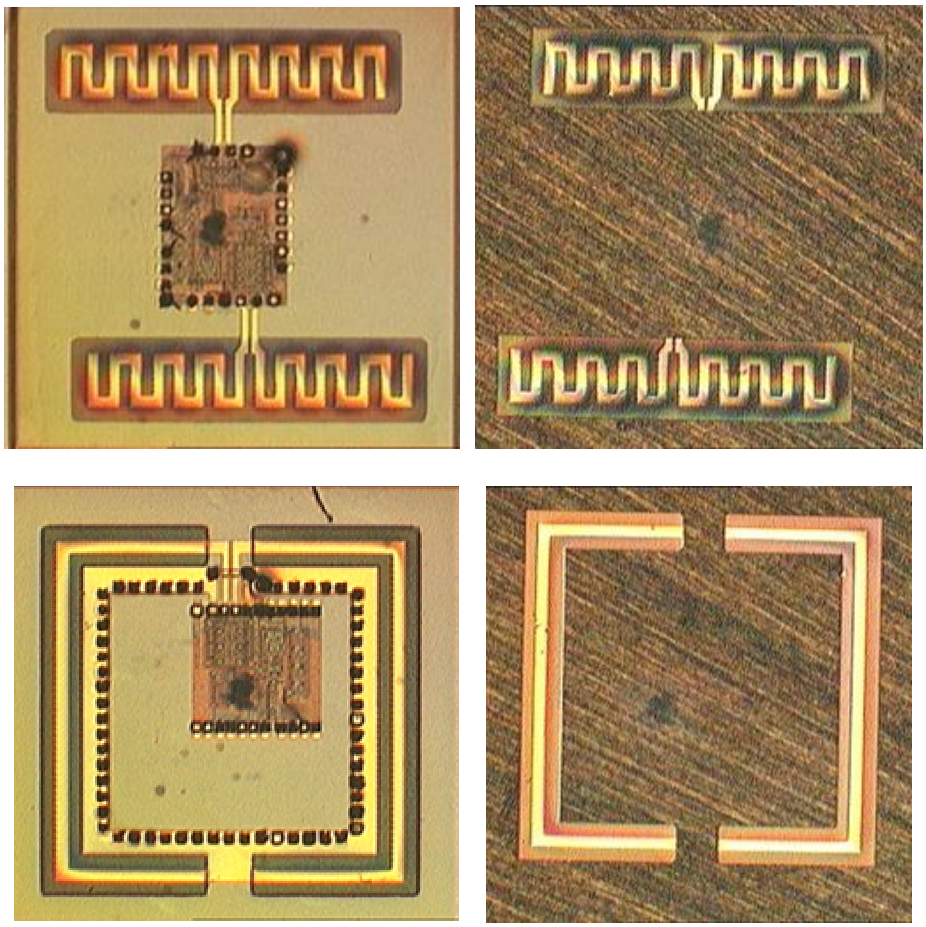


Figure 11. Examples of post-processed antennas with IC's (front and back sides)

Figure 11 indicates the pictures for two different types of post-processed antennas, front and back sides views. The structures are now under characterization.

In order to validate the post-processing technology, passive components without via interconnections to the IC's have also been realized and tested before and after fabrication. The corresponding low frequency noise measurement is indicated in Figure 12. No modification has been obtained, which permits to validate the entire post-process compatibility with the IC's.

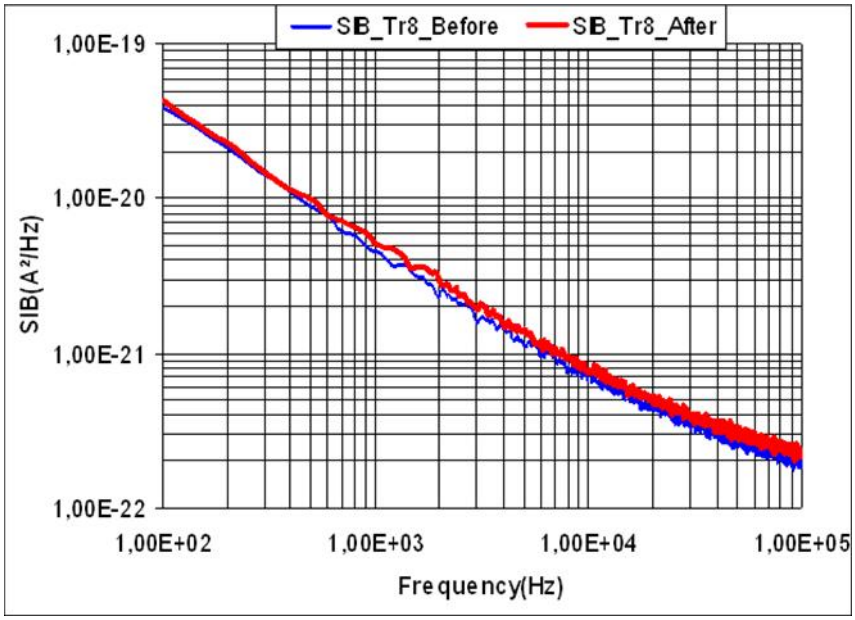


Figure 12. Low frequency noise measurement before and after post processing

CONCLUSION

In order to elaborate a compact RF communication module at 24GHz, a technological process based on the fabrication of suspended passive components on top of SiGe circuits has been developed.
This has been possible thanks to the use of polymer membrane instead of mineral ones, which exhibits too high temperature process and also strong stress levels.
The appropriate silicon etching technique has also been defined. Deep Reactive Ion Etching (DRIE) instead of a humid KOH bath has been chosen, because of its simple photoresist etching mask and its straight angles. These angles favour indeed the compactness of the entire RF module.
A first validation of the process has been done during the fabrication of antennas with trenches. These antennas have then been integrated to active devices, through an additional electroplating step to interconnect the post-processed antenna to the IC's.
Each critical technological step of this post-process has been validated in term of compatibility with the SiGe circuits. Both static and low frequency noise measurements have thus been used to control any behaviour modification of SiGe test transistors.

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