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A PLATFORM FOR EUROPEAN CMOS IMAGE SENSORS FOR SPACE APPLICATIONS

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I. INTRODUCTION

Both ESA and the EC have identified the need for a supply chain of CMOS imagers for space applications which uses solely European sources. An essential requirement on this supply chain is the platformization of the process modules, in particular when it comes to very specific processing steps, such as those required for the manufacturing of backside illuminated image sensors. This is the goal of the European (EC/FP7/SPACE) funded project EUROCIS. All EUROCIS partners have excellent know-how and track record in the expertise fields required. Imec has been leading the imager chip design and the front side and backside processing. LASSE, as a major player in the laser annealing supplier sector, has been focusing on the optimization of the process related to the backside passivation of the image sensors. TNO, known worldwide as a top developer of instruments for scientific research, including space research and sensors for satellites, has contributed in the domain of optical layers for space instruments and optimized antireflective coatings. Finally, Selex ES, as a world-wide leader for manufacturing instruments with expertise in various space missions and programs, has defined the image sensor specifications and is taking care of the final device characterization. In this paper, an overview of the process flow, the results on test structures and imagers processed using this platform will be presented.

II. CHIP ARCHITECTURE

A 2Kx2K backside imager with 8 different pixel variations of 14µm pitch has been designed using the 130nm CMOS/CIS process of imec. The conceptual architecture of the EUROCIS chip is presented in Fig. 1. A "digital control" block buffers the control signals to the row buffers, the column amplifiers and the analog output buffers. The "bias" block generates the bias currents and voltages needed for the analog readout. The "test block" includes some circuitry to perform basic tests and to access internal digital and analog signals for debugging purposes. The "digital row buffers" control the operation of the pixels during integration and readout. The "column amplifiers" read the pixel values row by row and perform correlated double sampling (CDS) to reduce the pixel kTC noise [Enz_PIEEE1996]. The "pixel array" consists of an array of 2048 rows by 2048 columns of pixels. The "analog output buffers" buffer and multiplex the output of the column amplifiers to 32 analog output pins. This means that 64 columns are multiplexed to one output buffer. The EUROCIS IC has analog outputs and no digitization is performed on-chip. Fig. 2 shows a simplified view of the IC's analog signal chain. Each column of pixels has its column amplifier, which includes the pixel's source follower bias current source.

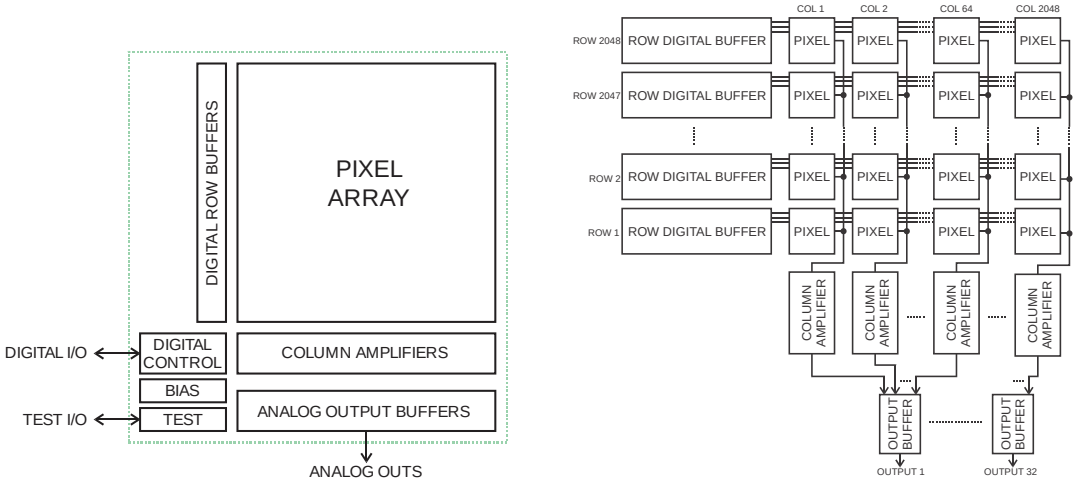

Fig. 1 EUROCIS chip: High level architecture (left) and IC analog signal chain (right).

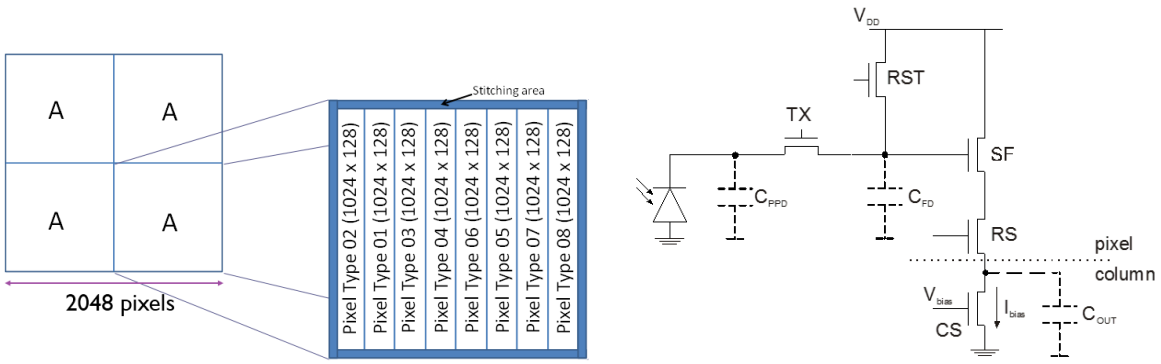

Fig. 2 Stitched pixel array consisting of 8 pixel variations (left), all based on the 4T design (right).

The pixel array occupies an area of approximately 30mm by 30mm. Since the lithography tool cannot illuminate such large area, the chip is built by "stitching" the different parts together. The photo mask only contains the sub-array "A" and the full array is formed by exposing this mask 4 times at the appropriate positions (see Fig. 2). The sub-array consists of 1024 by 1024 pixels selected out of 8 different pixel types, which are bundled in arrays of 1024 rows and 128 columns. All pixels are designed as 4T pixels with pinned photodiodes (PPD) as shown in Fig. 2. The different layout variations on the design are targeting different estimated full well charge (FWC) between 160ke$^-$ and 400ke$^-$. All pixel types are designed to meet space requirements in terms of radiation hardness by using radiation hard specific layout, e.g. enclosure type transistors.

II. CHIP MANUFACTURING

A. 0.13µm CMOS technology and backside process

Setting up a CIS (CMOS image sensor) process requires several additions and/or modifications to the standard CMOS process. The CIS industry standard today employs the so-called 4T-PPD pixel design [Fossum_JEDS2014]. Every pixel contains a low dark current PPD in addition to 4 special transistors. In order to maximize the pixel fill factor, 3 out of these 4 transistors can be shared between 2 to 4 pixels. Each of these transistors needs optimization of dimensions and process conditions in view of their specific task and operating condition. Also, the PPD needs to be optimized to minimize image lag at a designed-for pinning voltage.

The imec-internal CIS platform, running on a 200mm wafer size process facility, has been finalized during the EUROCIS project timeframe. Initial pixel process conditions and PPD/transistor dimensions were optimized using process and device simulations. A test design was made containing elementary test structures, including individual transistors, sheet resistivity structures, etc. as well as a variety of pixel designs organized in small pixel arrays.

The CIS process flow is discussed next. The Silicon substrates were designed for back-side illumination (BSI). The process flow consists of 13 front side (FS) modules and 3 BSI modules, depicted in Fig. 3. The front-end of line (FEOL) process consists of the shallow trench isolation (STI), the definition of the N and P wells, the PPD implantations and the gate and junction formation. The back-end of line process continues with pre-metal dielectric (PMD) deposition and the contact and inter-metal dielectric (IMD) formation. Subsequently, the necessary metal interconnect layers are created. At this phase also the MIM capacitors are formed. The final step is the passivation of the surface. At this stage the wafer includes all the circuitry and is ready for the backside processing. Pictures of a front side finished wafer and close up of a die are shown in Fig. 4.

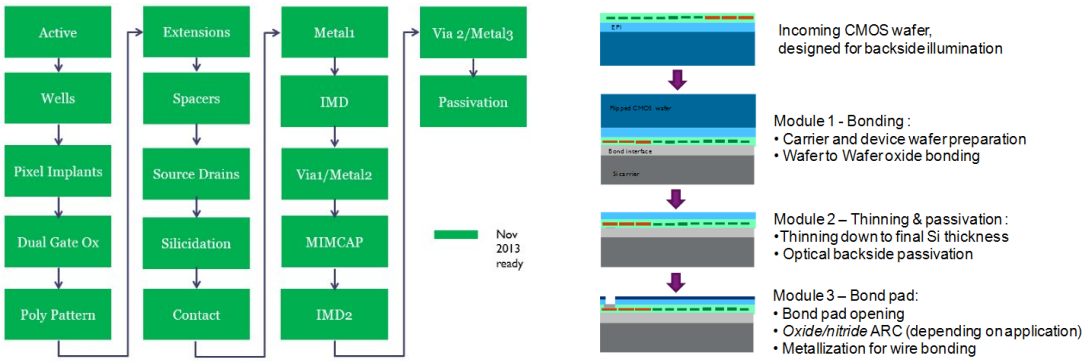

Fig. 3 Front side (left) and backside (right) process flow steps.

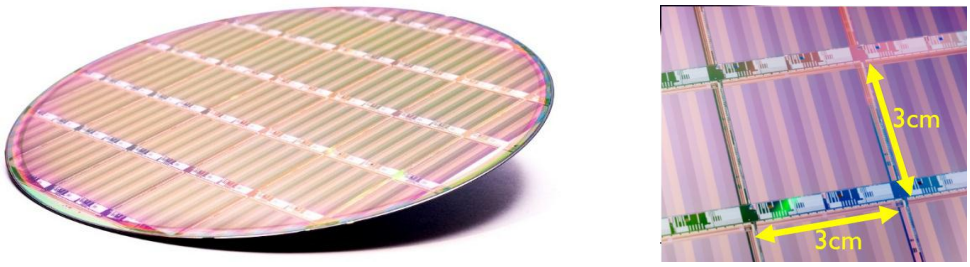

Fig. 4 Front side finished wafer and close-up of one die, pixel variations show as colour variations in columns.

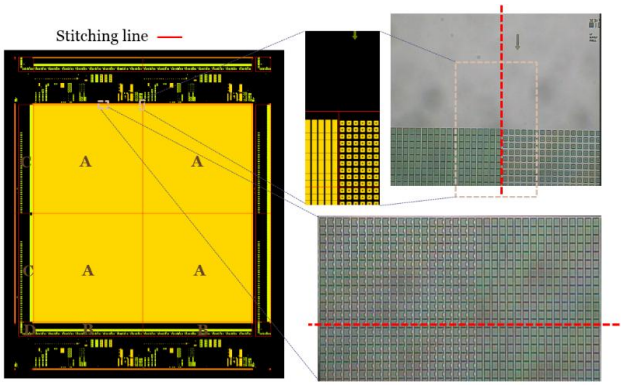

Fig. 5 Layout of the full chip and pictures of the stitched areas after processing.

A common BSI process flow [Cavaco_ECS2014], also shown in Fig 3, starts with the deposition of an oxide layer on the CMOS wafer. Chemical mechanical polishing (CMP) is used to planarize the deposited oxide. The wafer is then cleaned and plasma-activated before bonding. Subsequently, the wafers are bonded to a carrier wafer. Finally, the CMOS wafer substrate is thinned down until the non-sensitive bulk of the substrate of the CMOS wafer is removed.
Fig. 5 shows the layout of the full EUROCIS chip and the different stitched blocks are highlighted. No effect of the stitching was observed after inspection of the processed wafer. Wafer bonding is the most critical step of the BSI process. Pictures acquired using Scanning Acoustic Microscopy (SAM) (Fig. 6) show that the bonding is very good as no voids can be seen between the bonded wafers. After bonding the CMOS wafer was thinned down to 12µm. The final thickness for 4 different substrates is very close to the target value (blue line). Also, the total thickness variation (TTV) over the full wafer is below 1µm (red line).

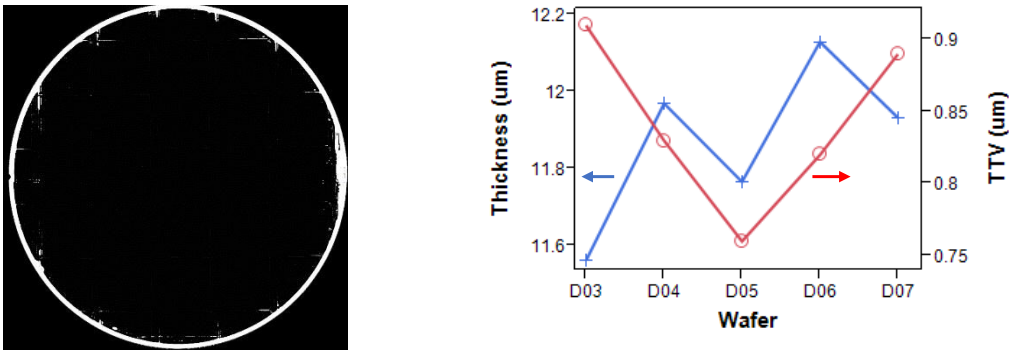

Fig. 6 SAM picture of 2 bonded wafers (left) and final thickness and thickness variation after thinning (right).

B. Backside Passivation
One of the critical issues in the fabrication of backside imagers is the need for passivation of the backside surface after the thinning step. A common technique to achieve that is by forming a backside junction, targeting 1) to achieve a dopant gradient induced back surface field to enhance sensitivity and 2) to passivate surface states to reduce dark current. To achieve these goals, the main requirements of the junction formation for image sensors backside passivation were drawn from recent literature [Huet_RTP2009, Wuu_IISW2009, Prima_IISW2009, Huet_RTP2010, Huet_IISW 2011], in combination with imec and LASSE know-how.

The backside junction if formed in two steps, the first step being ion implantation. The dopant profile should be as shallow as possible with low defects from implantation, especially near the dopant tail region. Therefore, a low dose implant is preferable to minimize implant defects. As demonstrated in [Wuu_IISW2009], although Ge or Si pre-amorphization is a well-known method to avoid dopant channeling and control the depth of shallow junctions, it should not be used since too much defects remain, even after laser annealing.
The second step of backside junction formation is laser annealing. Both melt and non-melt regimes were investigated as suitable methods to activate the implanted junction. In the melt regime, some diffusion of the dopants within the melted depth is observed with up to 90% activation rate for most implantation conditions. In the non-melt regime, the diffusion is negligible (within the SIMS measurement error) and the activation rate seems related to the number of shots, the energy density considered, as well as the dopant dose [Huet_IISW 2011].
The target specifications for the EUROCIS imager differs from traditional detectors in visible light as the EUROCIS spectrum is extended to near-UV. This requirement has a strong impact on the laser annealing conditions and has oriented our effort on sub-melting laser anneal instead of traditional laser anneal in melting phase. The final selection of sub-melting laser annealing conditions has opened several process solutions not accessible in traditional melting LTA. The best device performance can be achieved by overlapping standard laser beam size in the sub-melt condition. The main difference in terms of process requirement is that the full die exposure of the laser beam is not mandatory because the sensor area is annealed by overlapping smaller (standard) laser beams.
The uniformity of the scanning and the full die exposure techniques was studied using bare Si wafers. From the comparison of the surface resistance values after the laser annealing, it was clear that the scanning approach provides better uniformity within the sensor area. Additionally, the scanning approach is not depended on the design of the imager.

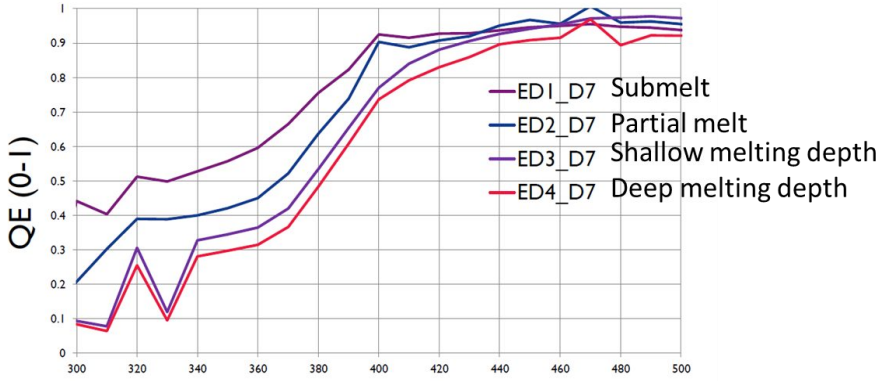

Fig. 7 Measured QE on a backside photodiode after different laser annealing conditions.

Next step was to investigate various laser annealing conditions on actual photodiodes and evaluate the effect on metrics like quantum efficiency (QE) and dark current (DC). A simple backside photodiode was used as a test vehicle, and the results are shown in Fig. 7. The main effect of the laser annealing is expected in the NUV region. This sub-melt condition creates minimal dopant diffusion compared to the partial, shallow or deep melt regimes. Finally, a comparison between single and multi-pulse approach showed that with the multi-pulse technique the junction quality is increased which can improve the pixel dark current. Pictures of a BSI completed full wafer and die are shown in Fig. 8,

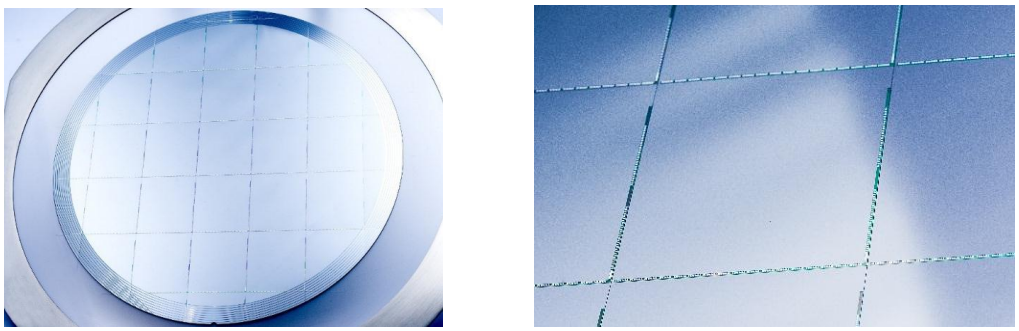

Fig. 8 Backside completed EUROCIS wafer and close-up of one die, before application of the ARC.

C. Antireflective Coating

The aim of an anti-reflection coating is to reduce reflection and maximize transmission on Silicon surfaces. In the EUROCIS project anti-reflection coatings have been developed for 1) broadband anti-reflection coatings for fused silica surfaces (e.g. camera windows) and 2) broadband anti-reflection coatings for backside illuminated imagers. Both the Vis/NIR band (400-1000nm) and the UV band (200-400nm) wavelength ranges are considered.

The anti-reflection coatings have been manufactured using e-beam evaporation in a Balzers/Evatec BAK760 system at a substrate temperature of 150ºC. To avoid pixel non-uniformity the process has been optimized to reduce spitting from the source. Additionally, the dies were inserted in a container for protection against particles originating from machine parts that are exposed to evaporated material. This container was opened after evacuation of the machine, and closed prior to venting. In this way the number of particles with a size between 1 and 5µm was reduced to 20–50/cm^2. No particles larger than 10µm were detected after coating. The effect of a 5µm particle on the sensitivity of a pixel is estimated to be approximately 10% while 1µm particles are expected to have a nearly negligible impact on pixels sensitivity.

Because of the high refractive index of silicon, the reflection broadband anti-reflection coated silicon is significantly higher than on glass or fused silica. But because of the not too large wavelength dependence of the refractive index, a satisfactory broadband coating can be made for the range of 400-1000nm.

Fig. 9 shows the calculated efficiency of uncoated silicon together with the measured efficiency of a Vis/NIR coated surface. The efficiency is defined as the fraction of light that enters the Silicon substrate and is calculated as 100% minus absorption and reflection. The anti-reflection coating consists of three layers. The materials used are HfO_2, SiO_2 and MgF_2. The anti-reflection coating improves the efficiency by 46% on average over the Vis/NIR band. The lower reflection results in a 84% reduction of the contribution of the detector to ghosting in optical systems.

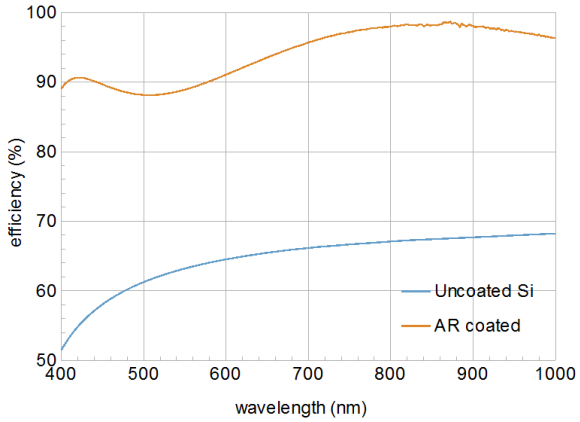

Fig. 9 Efficiency of Silicon with (orange) and without (blue) Vis/NIR anti-reflection coating.

Design and manufacture of UV anti-reflection coatings for Silicon faces two more challenges, especially in the ultraviolet range:

- No suitable high refractive index materials exist that are transparent below 225nm. Down to this wavelength HfO_2, with a refractive index of 2.1 can be used. Deeper in UV Al_2O_3, with an index of only 1.7, is the best option. This makes broadband AR coatings below 225nm impossible.
- The wavelength dependence of the refractive index and absorption coefficient of Silicon is strong and irregular, which means that increasing the bandwidth of the coating strongly reduces its performance.

This is illustrated in Fig 10. The HfO_2 based broadband coating has a much lower efficiency than the Vis/NIR coating, though the improvement over uncoated Silicon is still very significant down to 225nm. Below this wavelength, the absorption by HfO_2 results in a very poor performance. The Al_2O_3 based UV coating performs much better at short wavelengths, but its overall performance improvement compared to uncoated silicon is only half that of the HfO_2 coating.

From this analysis follows that anti-reflections for UV are best optimized for a specific application. Fig 10 also shows the measured efficiency of a coating optimized for the 270-350nm range, which is relevant for example for earth-observation missions. The coating consists of four layers of HfO_2 and SiO_2. Its performance is better than the broad band designs and is increased towards lower wavelength, somewhat compensating for the strongly decreased light intensity emerging from the earth.

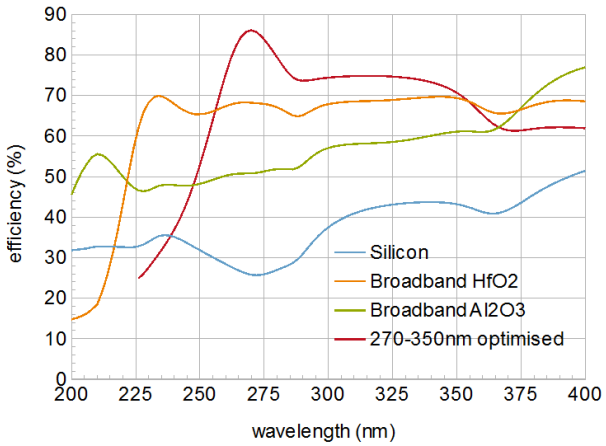

Fig 10 Simulated efficiency of a HfO_2 based (orange) and a Al_2O_3 based (green) broadband anti-reflection coatings and the measured efficiency (red) of a four layer AR coating optimized for the 270-350nm band, compared to the performance of uncoated Silicon (blue).

Coating of the imager dies is done after bond pad opening but before bonding of the dies. This means that coating of the bond pads has to be avoided. Since the distance between the bond pads and the pixels is 1.2mm, careful masking of the bond pads has been applied. For this purpose a dedicated interface that protects the bond pads and simultaneously minimizes contact with the die has been manufactured.
A picture of the coated die are shown in Fig 11. The light areas in these pictures are uncoated silicon area's which reflect relatively strong. The dark areas are coated with the Vis/NIR AR coating. The images shows that the bond pads have been effectively masked. The distance between the pads and the coated area is 0.45mm, which means that the entire pixel area has been coated.

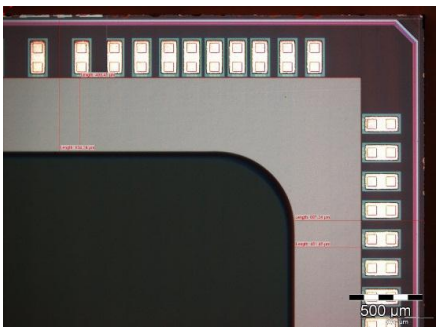

Fig. 11 Picture of an ARC coated EUROCIS imager die. The dark region is the AR coated area, the light region is uncoated silicon. The top and right of the picture show the uncoated bond pads.

D. Packaging and Testing
After completion, the EUROCIS chip needs to be connected to external electronics like the ADC board and the control and data acquisition boards/hardware. Typically, the chip is mounted on a package with socket and then on a specifically designed PCB. However, the large chip size and the non-standard pad layout (pads are located only on 2 sides of the chip) excluded the use of commercial packages. We adopted the Chip-On-Board (COB) approach: A specifically designed PCB onto which the EUROCIS chip can be mounted directly using wire bonding to the PCB pads, show in Fig. 12. At the time of writing the electrical evaluation was still ongoing.

Fig. 12 Backside COB packaged EUROCIS chip.

Selex ES is in charge of the specification definition and characterization steps of the project. The specification definition activity consisted of:

- Collect main optical requirements for space imagers for EO missions running or planned in the near future,
- Define the target imagers,
- Identify the goal requirements for the EUROCIS detector,
- Give a rationale of the choices carried out and
- Provide the necessary justification to this logic process.

The final activity is devoted to characterizing and qualifying the imager to demonstrate a technology readiness level equal to six (TRL 6). Before starting the test activity, some test jigs and ground support equipment have been designed and manufactured to mechanically interface the imager with the test facilities and to provide the electrical I/F with the imager. The tests foreseen on the detector can be divided into two main groups:

- Electro-optical characterization (functional and performance tests)
- Pre-qualification tests (Environmental tests).

The former group consists of all the necessary tests to characterize the detector performances; the tests include measurements of:

- Temporal noise,
- Output voltage offset
- Linearity error
- Charge To Voltage conversion factor, CVF
- Photo Response Non Uniformity, PRNU
- Quantum efficiency
- Spectral responsivity
- Dark current and Dark Signal non Uniformity, DSNU
- Modulation Transfer Function, MTF

The environmental tests include vibration and shock to assess the packaging maturity (ready for space) and thermal cycling to assess the roughness of the process (under stressed conditions). Between the environmental tests, a reduced set of electro-optical tests is foreseen. Fig. 13 shows the optical bench under preparation for the optical tests.

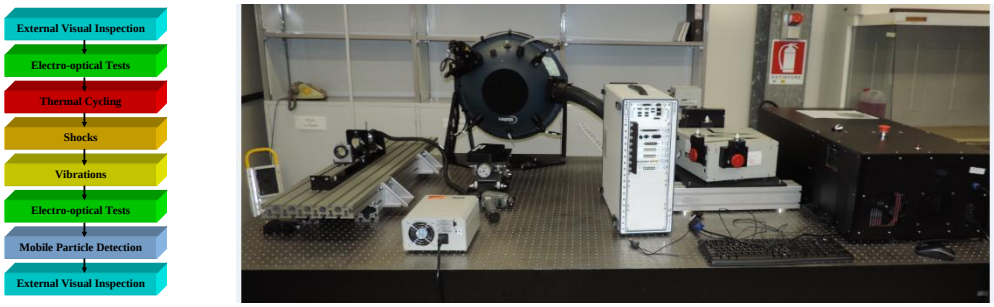

Fig. 13 Characterization sequence (left) and **o**ptical setup for EUROCIS (right).

III. CONCLUSION

A 2Kx2K backside imager with 8 different pixel variations of 14µm pitch has been designed using the 130nm CMOS/CIS process of imec. The chip, manufactured using stitched photolithography in the imec 200mm process line, went subsequently through the backside process. Part of this backside platform module is the laser annealing. Laser thermal annealing is considered to be the most appropriate low thermal budget approach to activate shallow Boron implants and achieving ultra-shallow junction depths at the backside of the thinned image sensor substrate. The next step was the optimization of the light coupling efficiency into the Si substrate by depositing appropriate optical layers onto the image sensor. Different materials and structures of antireflective coatings have been developed, targeting optimum sensitivity at NUV and visible wavelengths.

REFERENCES

[Enz_PIEEE1996] C. C. Enz et al, “Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization”, in Proceedings of the IEEE, vol.84, no.11, Nov 1996, pp.1584-1614.

[Fossum_JEDS2014] E. R. Fossum et al., “A Review of the Pinned Photodiode for CCD and CMOS Image Sensors”, in IEEE Journal of the Electron Devices Society, Vol. 2, No. 3, May 2014, pp. 33-43.

[Cavaco_ECS2014] C. Cavaco et al., “On the Fabrication of Backside Illuminated Image Sensors: Bonding Oxide, Edge Trimming and CMP Rework Routes,” in proceedings of ECS, 2014, Cancun, Mexico.

[Huet_RTP2009] K. Huet, et al., "Activation of ion implanted Si for backside processing by Ultra-fast Laser Thermal Annealing: Energy homogeneity and micro-scale sheet resistance," in 17th International Conference on Advanced Thermal Processing of Semiconductors, 2009, pp. 1-19

[Wuu_IISW2009] S. G. Wuu, et al., "A Manufacturable Back-Side Illumination Technology using Bulk-Si Substrate for Advanced CMOS Image Sensor," in *Proceedings of IISW*, 2009, Bergen, Norway.

[Prima_IISW2009] J. Prima, et al., "Improved colour separation for a backside illuminated image sensor with 1.4 µm pixel pitch," in *Proceedings of IISW*, 2009, Bergen, Norway.

[Huet_RTP2010] K. Huet, et al., "Full Device Exposure Laser Thermal Annealing: High performance and high yield junction formation process," in *18th International Conference on Advanced Thermal Processing of Semiconductors (RTP)*, 2010, pp. 50-52.

[Huet_IISW 2011] K. Huet, et al., "High Performance and High Yield Junction Formation with Full Device Exposure Laser Thermal Annealing," in *Proceedings of IISW*, 2011, Hakodate, Japan.