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HIGH SPEED TDI EMBEDDED CCD IN CMOS SENSOR

P. Boulenc[1], J. Robbelein[1], L. Wu[1], L. Haspeslagh[1], P. De Moor[1], J. Borremans[1], M. Rosmeulen[1]
[1]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
Email: pierre.boulenc@imec.be, Phone: +32 16 28 15 44

I. ABSTRACT:

This paper reports on a Time Delay and Integration image sensor System-on-Chip realized in an embedded CCD process. The integration of single-poly CCD modules into a standard 0.13µm CMOS process is discussed. The technology performance has been evaluated using dedicated test structures. Next, a prototype TDI imager with 5µm pixel pitch, 512 rows and 1024 columns was designed, manufactured and characterized. Charge Transfer Efficiency greater than 0.9999 up till very high line rates of 400kHz was recorded.

II. INTRODUCTION:

Despite today's dominance of CMOS Images Sensors (CIS), the unique feature of noiseless charge transfer still ensures superior performance of CCD image sensors in a number of demanding applications. One such application is Time Delay and Integration (TDI) imaging, the preferred line scanning technique used in industrial inspection and earth observation. CCD-based implementations of TDI imaging typically result in higher SNR and lower data rate as compared to their digital-TDI CIS-based counterparts. These are decisive benefits in a growing field of high-speed and light-starved applications.

Incumbent CCD technologies suffer from low level of integration, requiring multiple Integrated Circuits (IC) for imaging, control and read-out, complicating high-speed, low-noise and low-power operation. A CCD module with CMOS-rated voltages has been developed and embedded in standard CMOS, bringing the benefits of System-on-Chip (SoC) integration to CCD imaging. Building on previous technology demonstrations [1], this work presents improved performance and application in a highly-integrated TDI image sensor.

III. EMBEDDED CCD TECHNOLOGY:

The embedded CCD in CMOS (eCCD) platform was realized by adding a few process modules to a standard 0.13µm CMOS process flow containing dual gate oxide standard nMOS and pMOS transistors (1.2 and 3.3V). Dedicated well and junction implants for the CCD elements and readout transistors have been used to ensure CMOS compatible operating voltages (Fig. 1).

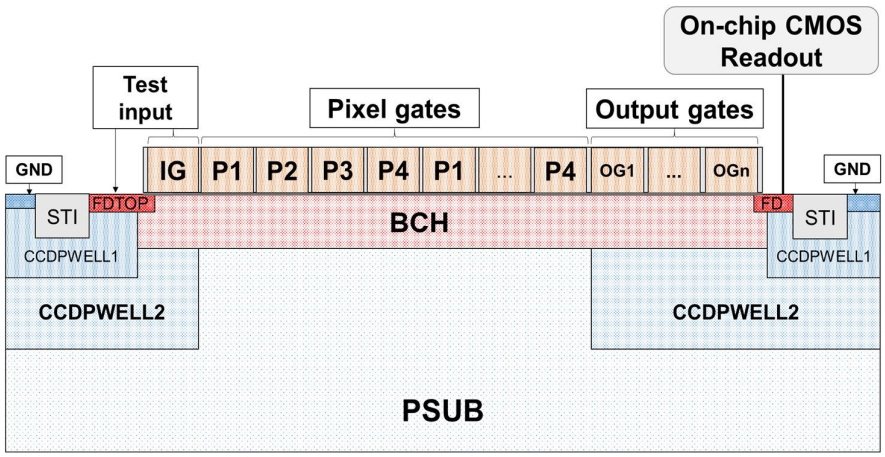

Fig. 1. Schematic cross-section of a CCD column embedded into a standard dual gate oxide 130nm CMOS technology. the CCD buried channel (BCH) and floating diffusions (FD) are dedicated implantation steps.

The CCD pixels optionally include a lateral Anti-Blooming (AB) scheme, the correct operation of which is demonstrated in Fig. 2. At high CCD gate bias, the electrostatic potential maximum (defining the buried channel) moves towards the Silicon / Gate-Oxide interface. As a consequence, electrons interact with the interface traps leading to both Charge Transfer Efficiency (CTE) degradation and Full Well Capacity (FWC) loss [2]. Activating the AB gate drains excess electrons, preventing them from reaching the Silicon / Gate-Oxide interface.

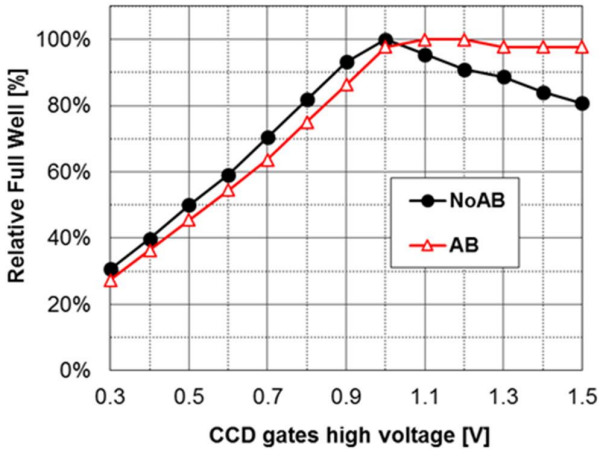

Fig. 2. Verification of Anti-Blooming function. At high CCD gate bias, electrons accumulate at the Silicon / Gate Oxide interface leading to FWC loss. Surface charge is drained by AB, preventing the FWC loss.

Advanced single-poly gate patterning is employed to enable narrow poly-to-poly spacing (Fig. 3) for the 4-phase 5µm pitch pixels. Imec's eCCD process platform is also fully compatible with Back-Side Imaging (BSI) which can be included by means of additional steps at the end of the production process.

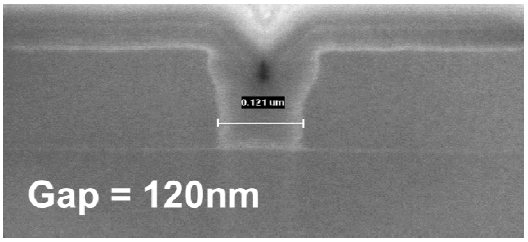

Fig. 3. Cross-section SEM image of 120nm poly-to-poly gap realized using the dedicated single-poly eCCD gate module.

Dedicated test structures are used to determine the dark current for various poly-to-poly gap widths. These structures consist of two CCD columns. Each bottom FD is connected to a Reset and a Source-Follower transistors allowing to monitor the output signal versus time through a scope probe. Dark current for gaps between 100nm to 180nm were measured at room temperature and show almost no variation with respect to gap width. The presence of Anti-Blooming is found to slightly lower the dark current by draining part of the generated electrons.

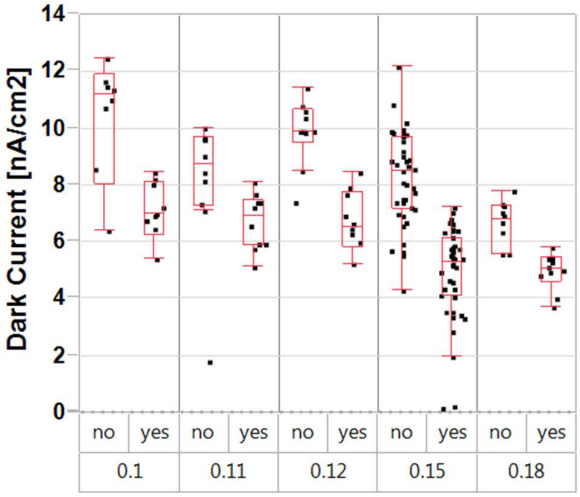

Fig. 4. Dark current measured on CCD test structures at 25˚C versus poly-to-poly gap (in µm). Yes/no indicates the presence/absence of AntiBlooming scheme in the test structure.

The same structures are also used to record the Photon Transfer Curve (PTC) depicted in Fig. 5. From the PTC, a Conversion Gain (CG) of 23µV/e- and a FWC around 17400 electrons with a noise floor of 20 electrons have been determined.

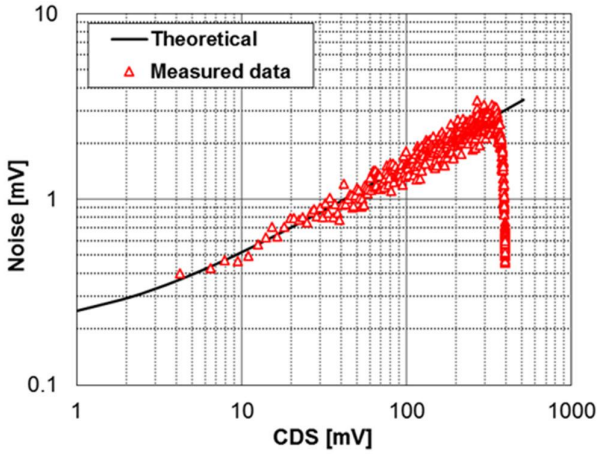

Fig. 5. CCD test structure Photon Transfer Curve demonstrating proper functioning of the eCCD technology.

IV. TDI PROTOTYPE:

A 512x1024 pixel TDI image sensor (Fig. 6 left) has been designed and manufactured using the presented eCCD technology. On-chip CMOS logic and CCD drivers with slew rate control (Fig. 6 right) drive the 1024 column 4-phase CCD array, with 512 rows and stage selection. Analog column-parallel readout samples reset and video signals, serializes and buffers the output to an off-chip ADC. The sensor uses CMOS-rated supply voltages up to 3.3V and a negative supply of -1.3V, while being fully compatible with standard CMOS readout.

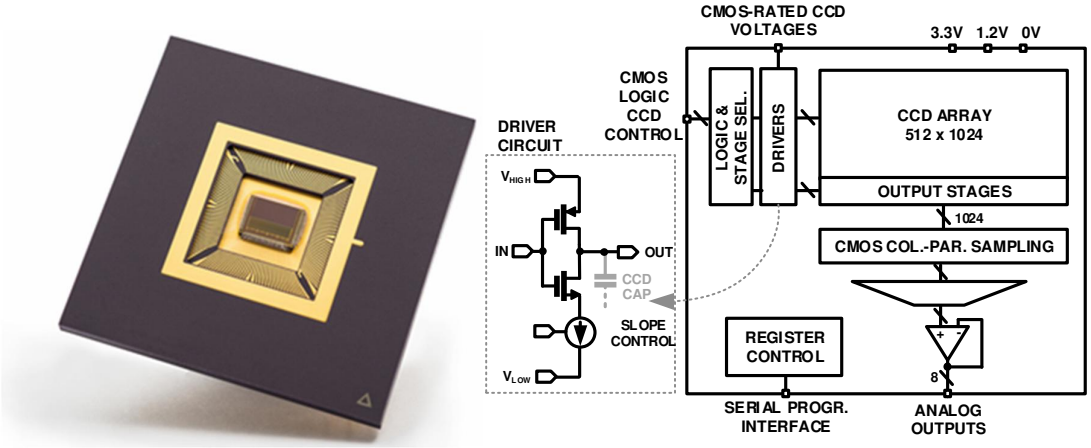

Fig. 6. eCCD TDI packaged prototype (left) with the corresponding circuit block diagram (right) including CCD pixel array and CMOS-based on-chip logic, row drivers with slew rate control, column-parallel sample-and-hold, serializer and buffers.

CTE has been measured [3] individually per column and is greater than 0.9999 up till 400kHz (Fig. 7). Peak CTE value of 0.99995 is reached between 50kHz and 400kHz, demonstrating the high-speed performance capability of imec's eCCD platform. In this prototype, the CCD column sampling circuits share a limited amount of buffers. The resulting total readout bandwidth is thus limiting the full-frame line rate to 50kHz. This can be improved thanks to higher circuit integration like column level Analog to Digital Converters (ADC).

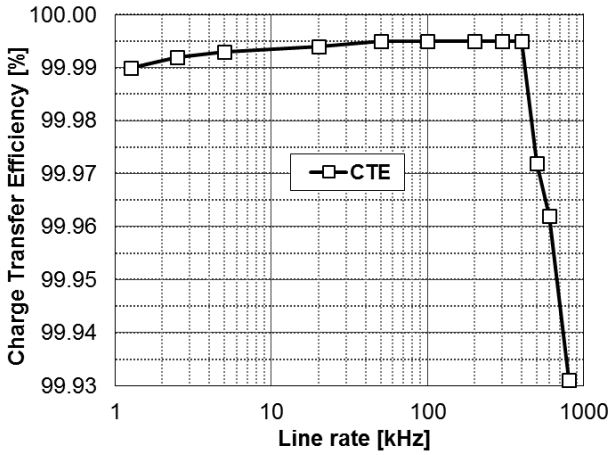

Fig. 7. Charge Transfer Efficiency (CTE) as a function of the line rate at 50% FWC. Measurement is performed on a column of the TDI SoC with 110nm poly-to-poly gap width.

Analysis of the full sensor PTC (Fig. 8) confirms the test structures data. FWC is equal to 18000 electrons with activated AB, CG is 1 Digital Number (DN) per electron and noise floor is 20 electrons including electronic circuitry readout noise.

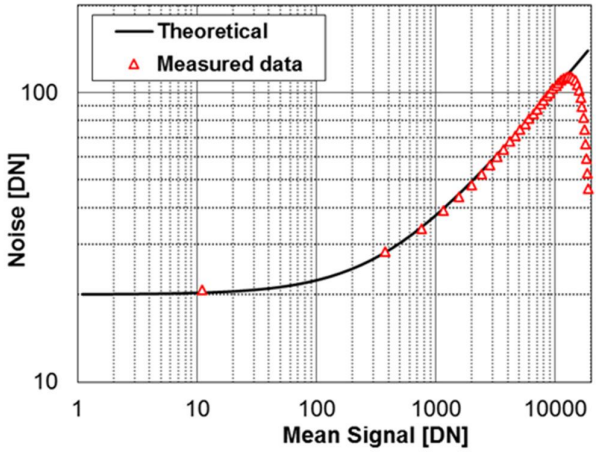

Fig. 8. Dark current histogram at 25˚C for the same sensor (right).

The sensor shows a x2 lower dark current (Fig. 9) compared to the test structures. The absence of Shallow Trench Isolation (STI) in the sensor significantly improves the dark current compared to the test structures which have STI along one side of each CCD column.

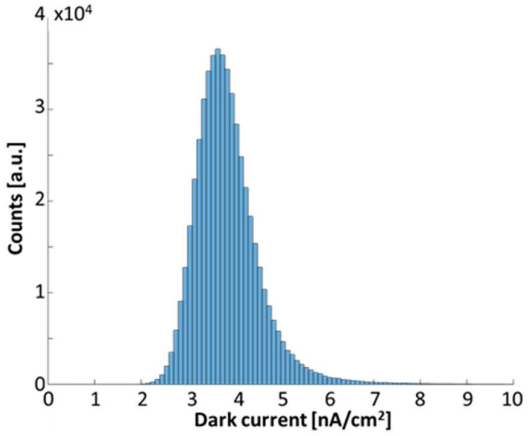

Fig. 9. Dark current histogram at 25˚C for the same sensor as in Fig. 8.

Fig. 10 presents a still-image collected by the sensor with an appropriate clocking sequence:

- firstly, the sensor is emptied by clocking the gates constantly at 50kHz; this corresponds to a flush sequence;
- then, the clocks are stopped for a given integration time; this is done when 2 CCD gates are at low bias and 2 CCD gates are at high bias, forming an electrostatic potential well where the photo-electrons are collected; this is the integration sequence;
- finally, the sensor is clocked at 50kHz and the electron packets are read; this is the second flush sequence.

Subtracting a dark current frame of the same integration time and the mean signal collected during the first and second flush sequences allows to get to the light generated electrons only.

Fig. 10. Still-image (512x1024) produced by projecting a diapositive onto the sensor and using a flush-integrate-flush sequence with 20ms integration time. The black rectangular shapes on the left, top and right of the picture are caused by the use of metal shields, one can see two 4x4 pixels pinholes in the right black rectangle.

A TDI image is presented in Fig. 11. This picture has been obtained by imaging playing cards installed on a conveyer belt. The sensor line rate has been set at 7kHz to match the conveyer belt speed. The eCCD TDI sensor features a stage selection which splits the sensor in 2 blocks of respectively 504 and 8 rows in order to adjust the amount of collected charges for low speed or high illumination levels. Only the last 8 pixel rows have been used to build this TDI image, the rest of the pixel rows moving their charges towards the floating diffusion at the top of the CCD columns.

Fig. 11. TDI image (1024x2500 pixels) produced by scanning playing cards on a conveyer belt at 7kHz.

Table 1 compares the performance of this device to results published in literature. Comparable FWC per unit of area, Conversion Gain and noise figures are obtained. This work differentiates in terms of high speed operation and imager resolution. Moreover, the sensor is operated with standard CMOS compatible voltages only, allowing a high level of System-on-Chip integration (like on-chip ADC) and low power consumption.

Table 1. Comparison of parameters for different published CCD-in-CMOS technologies.

	imec	[4]	[5]
Technology	130nm	180nm	150nm
Array size	1024	64	128
Number of rows	512	40	64
Pixel size	5µm	13µm	7.5µm
Full well	18ke-	110ke-	92ke-
Conversion gain	25uV/e-	11uV/e-	10–15uV/e-
Electronic noise	20e-* *incl. read noise	N/A	~20e-
Dark Current at RT	3.5nA/cm^2	12nA/cm^2	0.3nA/cm^2
Full-Frame line rate	50kHz	N/A	15kHz
Max line rate	400kHz	N/A	N/A
CTE	>0.9999	0.9998	0.99999
Supply voltage Max	3.3V	>3.6V	N/A
Integrated drivers	YES	NO	N/A
Column readout	YES	N/A	N/A

It should be noted that CTE requirements can be relaxed using column-parallel readout in eCCD technology, since there is no high-speed horizontal CCD shift register required as in classical CCDs. All serialization occurs in the voltage (or digital) domain.

V. CONCLUSIONS:

This work demonstrated the operation of a System-on-Chip CCD-based TDI imager implemented in a baseline 130nm CMOS process. Imec's eCCD technology exhibits a high line rate of 400kHz, a small pixel size of 5µm, acceptable CTE of 0.99995 and noise floor of 20 electrons, suitable for high-speed imaging applications. In the context of space imagers development, eCCD is a promising alternative to classical TDI CCD sensors and allows higher level of System-on-Chip integration. Finally, the sensor is fully operated with CMOS rated voltages enabling low-power imaging in a demanding environment.

VI. ACKNOWLEDGEMENTS:

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