Front-end readout ASIC for charged particle counting with the RADEM instrument on the ESA JUICE mission

Timo A. Stein[*a,b], Philip Påhlsson[a], Dirk Meier[a], Amir Hasanbegovic[a], Hans Kristian Otnes Berge[a], Mehmet Akif Altan[a], Jörg Ackermann[a], Bahram Najafiuchevler[a], Suleyman Azman[a], Jahanzad Talebi[a], Alf Olsen[a], Codin Gheorghe[a], David Steenari[a], Petter Øya[a], Tor Magnus Johansen[a] and Gunnar Maehlum[a]

[a]Integrated Detector Electronics AS (IDEAS), Gjerdrums Vei 19, 0484 Oslo, Norway
[b]Department of Physics, University of Oslo, Sem Sælands Vei 24, 0371 Oslo, Norway

ABSTRACT

The detector readout for the Radiation-hard Electron Monitor (RADEM) aboard the JUpiter ICy moons Explorer (JUICE) uses a custom-made application-specific integrated circuit (ASIC, model: IDE3466) for the charge signal readout from silicon radiation sensors. RADEM measures the total ionizing dose and dose rate for protons (5 MeV to 250 MeV), electrons (0.3 MeV to 40 MeV) and ions. RADEM has in total three chips of the same design: one chip for the proton and ion detector, one for the electron detector, and one for the directional detector. The ASIC has 36 charge-sensitive pre-amplifiers (CSA), 36 counters of 22-bits each, and one analogue output for multiplexing the pulse heights from all channels. The counters count pulses from charged particles in the silicon sensors depending on the charge magnitude and the coincidence trigger pattern from the 36 channels. We have designed the ASIC in 0.35-µm CMOS process and an ASIC wafer lot has been manufactured at AMS. This article presents the ASIC design specifications and design validation results. The preliminary results from tests with bare chips indicate that the design meets the technical requirements.

Keywords: ASIC, RADEM, IDE3466, readout, charged particle detection, coincidence counting, radiation monitor, JUICE.

1. INTRODUCTION

1.1 ASIC requirements and application

The IDE3466 ASIC has been developed for the front-end detector readout in the Radiation-hard Electron Monitor (RADEM; [1], [2]), aboard the ESA JUpiter ICy moons Explorer (JUICE, [3]). The ASIC will be used in the proton and ion detector, the electron detector and in the directional detector. The electron and proton detectors are designed from a stack of alternating diodes and absorbers, which allow one to derive the particle energy from the depth-of-interaction in the detector stack by measuring the coincident pattern of triggers received from the diodes. The ASIC has 36 charge-sensitive pre-amplifiers (CSA) each AC-coupled to a radiation sensor diode, 36 counters of 22-bits each, and one analogue output for multiplexing the pulse heights from all channels. The ASIC can be operated with an external microcontroller for programming the ASIC registers and reading out the counter data in regular intervals via a serial interface. Out of the 36 channels, 32 channels have high-gain pre-amplifiers while the other 4 channels have 10 times lower gain pre-amplifiers. The high-gain channel counters trigger on charge exceeding threshold charge that is programmable in the range from 2.2 fC to 100 fC and from 15 fC to 1 pC. The low-gain channel counters trigger on charge from 260 fC to 26 pC. With these parameters the RADEM detector system is sensitive to electrons from 0.3 MeV to 40 MeV, and protons from 5 MeV to 250 MeV and helium to oxygen ions in the range from 0.1 to 10 MeVcm^2/mg.

[*] e-Mail: timo.stein@ideas.no; phone: +47-67414990; URL: http://www.ideas.no.

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1.2 ASIC design heritage

The RADEM ASIC IDE3466 is a successor of the IDE3465 (VATA465) ASIC, which has been developed for the ESA Next Generation Radiation Monitor (NGRM; [4], [5]). IDEAS has designed ASICs for other space missions, and some design heritage for space projects is summarised in [6], [7]. The IDE3466 for RADEM includes new design elements for triple-modular redundant registers, parity error detection, coincidence and pattern unit with counters, and a latch-up detection circuit. For other projects, we have manufactured test devices and validated the design with respect to heavy ions. We have measured a single-event-upset (SEU) threshold of 50 MeVcm^2/mg and we did not observe any latch-up up to the maximum tested energy of 135 MeVcm^2/mg [8].

1.3 Readout of silicon diode radiation sensors

Figure 1 shows the system block diagram with silicon diode radiation sensors, the integrated circuit (ASIC), and the readout system. All diodes are fully depleted by an electric field that is due to +70-V bias voltage applied to every cathode. Charged particles traversing the diode generate charge carriers that move in the depleted bulk and induce an electric current in the electrodes. This current can be measured via the coupling capacitor that connects every anode to a charge-sensitive pre-amplifier input. The bias resistor defines the 0-V anode potential and conducts the diode leakage current. The ASIC has a total of 36 channels: 4 low-gain channels (LG) and 32 high-gain channels (HG). The channel input design is optimised for the readout of the anode signal, that is for charges of positive polarity. The nominal sensor and coupling parameters are: 10-pF diode capacitance, 470-pF coupling capacitance, and 2.2-MOhm bias resistor.

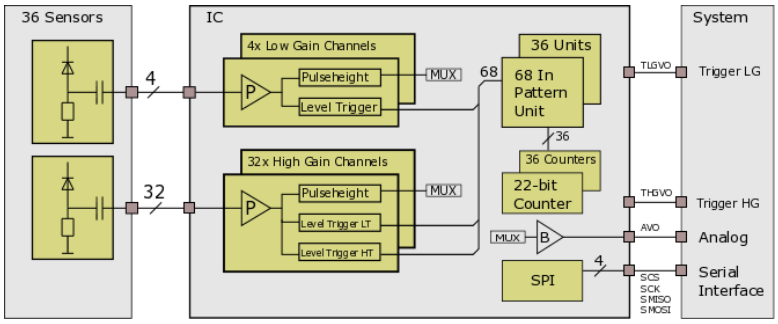

Figure 1: Block diagram with radiation sensors (left), the integrated circuit (ASIC, centre), and readout system (right).

Every ASIC channel has one charge-sensitive pre-amplifier (P), and analogue processing circuits for pulse-height spectroscopy and level comparators (triggers). The pulse heights can be multiplexed (MUX) to an analogue buffer (B) and read out sequentially by the system. The level triggers feed 36 coincidence pattern units, and 36 digital counters (one counter per pattern unit). Each high-gain channel has two comparators to discriminate pulse heights and to generate two digital pulses when the pulse height exceeds any of the programmable thresholds. Low-gain channels only have one comparator to generate one digital pulse. Every comparator threshold can be programmed individually with a 10-bit digital-to-analogue converter (DAC). Their threshold range can be programmed globally with another on-chip DAC (*DAC_GLOBAL_GAIN*). The ASIC can be operated in two different modes:

1. **Pulse-height spectroscopy:** the ASIC allows one to measure simultaneously in all channels the amount of charge that is generated when charged particles interact in the radiation sensors. The system reads out the pulse height (analogue voltage) via the AVO signal, which is digitised by an external analogue-to-digital converter (ADC).
2. **Coincidence pattern counting:** the ASIC counters increment depending on the programmed settings and the combination/pattern and magnitude of charges in the radiation sensors. The system regularly reads out the counters via the serial peripheral interface (SPI). It is possible to program individually each coincidence unit for triggering on a specific pattern. A special case is the single-channel analyser (SCA), which can be programmed with the two thresholds in high-gain channels. A SCA has two thresholds and a counter, which increments when the pulse height is in between the two thresholds. The coincidences conditions among the radiation sensors are programmable at power-up and re-programmable during operation when needed.

2. ASIC DESIGN SPECIFICATIONS

2.1 Overview

Table 1 summarises the ASIC features, and Figure 2 shows the ASIC block diagram.

Table 1: ASIC features and preliminary performance results.

4 low-gain channels (LG), charge-sensitive inputs Spectroscopy up to +20.8 pC, ENC ≈ 33000 e + 3 e/pF 1 threshold, 10-bit linear prg. from 260 fC to +22.8 pC, 260 fC lowest threshold above noise 1 trigger logic OR digital output
32 high-gain channels (HG), charge-sensitive inputs Spectroscopy up to +2.2 pC, ENC ≈ 3320 e + 9 e/pF 1 low threshold (HGLT), 10-bit linear prg. from 1.2 fC to +0.1 pC, 2.2 fC lowest threshold above noise 1 high threshold (HGHT), 10-bit linear prg. from 15 fC to +1 pC, 15 fC lowest threshold above noise 1 trigger logic OR digital output
Energy-resolved counting 36 digital counters read out via serial peripheral interface (SPI) 22-bit Gray code counters 1 Mcps / HG-channel count rate for 600 fC input charge 100 kcps / LG-channel count rate for 10 pC input charge 68-to-1 programmable coincidence pattern logic for every counter
Pulse-height (charge) spectroscopy Analogue mux. output from all channels
150 mW power typical operation, 240 mW power worst-case register settings
SEL/SEU radiation hardened (triple-modular redundant, parity check, enclosed layout structures)

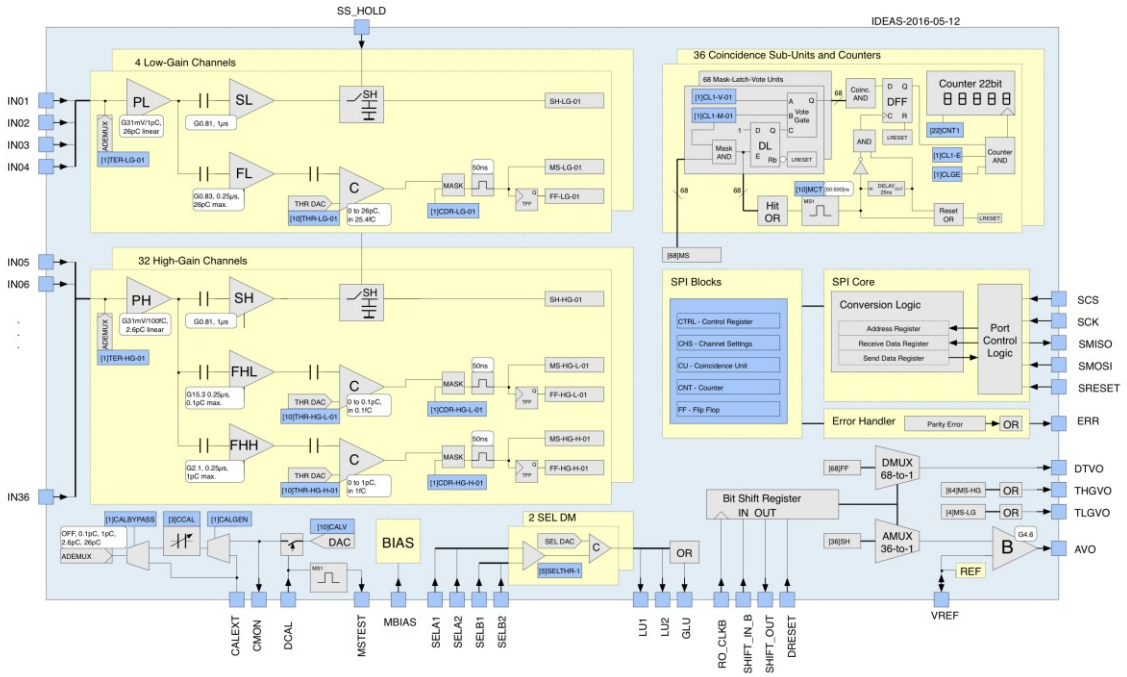

Figure 2: ASIC block diagram.

The ASIC operates with two positive voltage supplies (V_{REF} = +1.8V and V_{DD} = +3.3V) and one external reference bias current (MBIAS = 300 µA). The total power consumption is 150 mW during typical operation in counting mode. The ASIC has a serial peripheral interface (SPI) for programming its register settings and for the digital data readout. All amplifier inputs are protected by diodes against over-voltage and electro-static discharge (ESD). The following paragraphs describe details of the design specifications.

2.2 Analogue front-end

The analogue front-end contains charge-sensitive pre-amplifiers, shapers, and comparators. Each channel has a charge-sensitive pre-amplifier (CSA) with unity gain output buffer (Figure 3). The voltage amplitude V (pulse height) at the output of the CSA is proportional to the time integral of the input current I, i.e. the charge Q. The ratio of the pre-amplifier output voltage V over the input charge Q is the pre-amplifier gain $G_P = V / Q$, which is to first order equal to $G_P = 1/C_f$. The low-gain channels have one fixed 25-pF and high-gain channels have two parallel 1.25-pF feedback capacitors where the second can be enabled or disabled. The gain of the pre-amplifier and output buffer is 31 mV/1 pC for the low-gain channels and 31 mV/100 fC for high-gain channels. The pre-amplifier DC feedback is a metal-oxide-semiconductor (MOS) transistor, which determines the de-charging slope after current integration, and thereby contributes to the noise and rate capability. The pre-amplifier output returns to baseline in less than 40 µs for input charges Q smaller than 20 fC. Figure 4 shows the shaper principle, which is the same for all shaping amplifiers in the ASIC. Each channel has a slow shaper for pulse-height spectroscopy and fast shapers for triggering and counting. The logic OR from the trigger is used to initiate the readout sequence of pulse heights from slow shapers. All shapers are of CR-RC type first-order, semi-Gaussian band-pass filter, with a shaping time of $\tau = R_{fb} \times C_2$. The shaper gain G_S is approximately $G_S = C_1/(eC_2)$, and the gain values are noted next to the shapers in Figure 2. The slow shapers have 1-µs shaping time and the fast shapers have 0.25-µs shaping time.

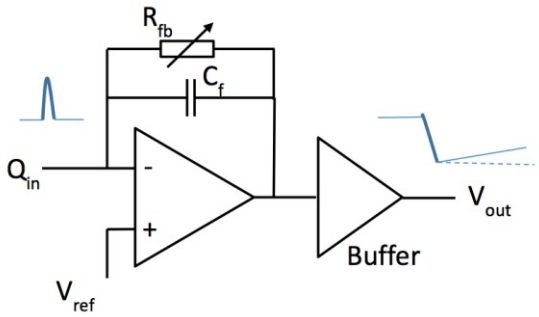

Figure 3: Pre-amplifier principle.

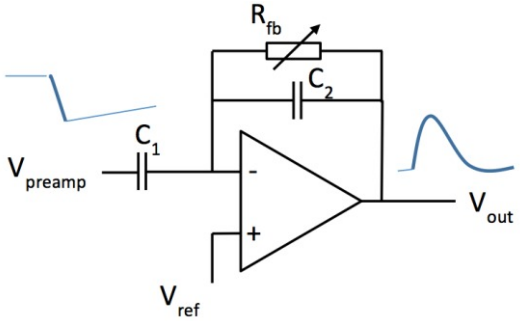

Figure 4: CR-RC shaper principle.

Each channel slow shaper output has a track-and-hold unit. The hold time is controlled externally for all channels simultaneously by SS_HOLD. The capacitor tracks the slow shaper output and its value is held when the SS_HOLD becomes active high. The held values can be read out through the analogue multiplexer. The SS_HOLD signal should be applied externally at time when the slow shaper output signal reaches its peak value. The slow shaper output signal peaks about 1.3 µs after the current pulse enters the preamplifier input, and this is when the SS_HOLD signal should be applied.

2.3 Pulse-height spectroscopy and analogue readout

Figure 5 shows the timing diagram for the pulse height readout from all channels following the current integration and triggering on the pulse height. The time sequence items (cf. Figure 5) are described below:

1. Optional: The external system resets the readout registers with DRESET (1). The reset is optional, and only necessary if a previous operation left any of the readout shift registers active.
2. Ionising radiation generates a current pulse in the radiation sensor that is connected to channel N (2).
3. The trigger of channel N and one of the trigger-OR (THGVO or TLGVO) fires (3).

4. The external system activates SS_HOLD sometime after the current pulse causes the trigger (4). The exact time depends on the peaking time, which can be determined experimentally. The SS_HOLD should be activated at the peak of the shaped pulse. At the rising edge of SS_HOLD the shaper output is sampled and held. A readout sequence can now be started.
5. The external system activates SHIFT_IN (5).
6. The external system resets SHIFT_IN (6). The SHIFT_IN must not be high for more than one RO_CLK clock cycle. DRESET must not be high during the rest of the readout, unless one wants to reset the readout.
7. The external system generates a rising edge at RO_CLK (7).
8. The sampled pulse height of the first low-gain channel (LG1) appears at AVO and the trigger output of channel LG1 appears at DTVO. This state is valid for two RO_CLK clock periods (8).
9. After 8 clock cycles, the low-gain channel readout is finished and the high-gain readout begins (9). The 9th clock cycle provides the trigger output for the high-gain low-threshold trigger (HG1-LT) on the DTVO output. Simultaneously, the pulse height of the first high-gain channel (HG1) appears on the AVO output. The 10th clock cycle provides the trigger output for the high-gain high-threshold trigger (HG1-HT) on the DTVO output. The pulse height of the first high-gain channel remains at AVO during the 10th clock cycle as well. Applying another clock cycle starts the readout of the next high-gain channel (HG2).
10. At the 66th RO_CLK clock cycle, the last high-gain channel readout is started (HG32), and at the 68th RO_CLK clock cycle, the readout of all channels is finished (10).
11. At the 68th RO_CLK clock cycle, SHIFT_OUT goes high (11), and goes low after the next clock cycle.
12. Applying a 69th clock cycle or a DRESET resets/clears the readout registers (12).

The RO_CLK maximum frequency is designed for 1 MHz, which implies 68-µs dead time for reading out the pulse height from all 36 channels. To reduce dead time one can pre-clock the analogue multiplexer to LG01, wait for the event to occur, and carry out the readout sequence for all channels as shown below.

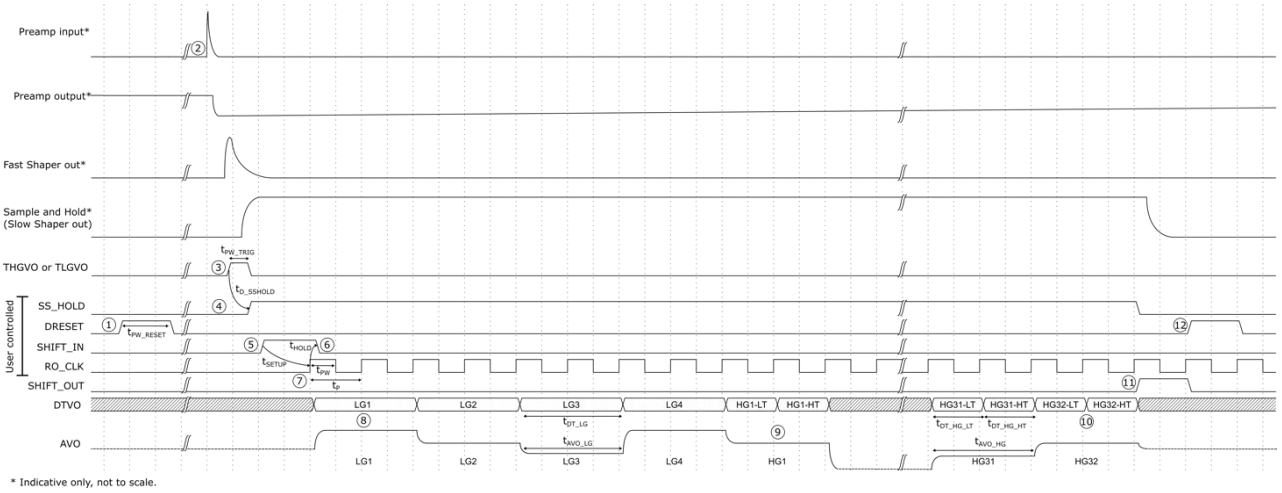

Figure 5: Timing diagram of the track-and-hold readout from slow shapers.

2.4 Coincidence pattern counting

The coincidence pattern unit has 36 identical sub-units. Each sub-unit receives the mono-stable trigger outputs from all analogue channels: two outputs from each HG channel and one output from each LG channel, which is a total of 68 digital signals. Each sub-unit has one 22-bit Gray-code counter. Each counter value is readable through the serial peripheral interface (SPI). Figure 6 illustrates the operation of the coincidence pattern sub-unit. The example shows two digital pulses out of 68 possible pulses. The first pulse starts the coincidence time. The pulses that occur during the duration of the coincidence time constitute the digital pattern that is evaluated at the end of the coincidence time. A pulse width from a non-retriggerable mono stable (MCT) defines the duration of the coincidence time. The mono stable pulse width is logarithmically programmable in the range from about 50 ns to about 622 ns as shown in Figure 7.

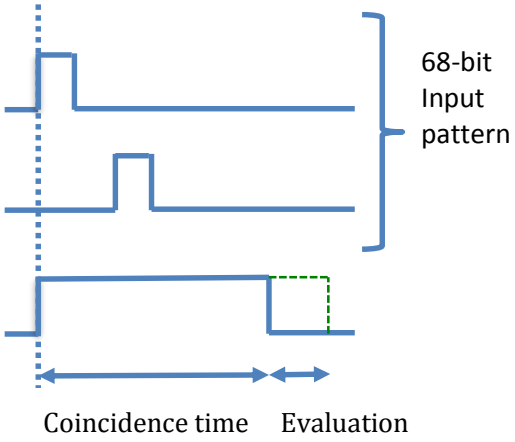

Figure 6: Illustration of two digital pulses within the coincidence time duration.

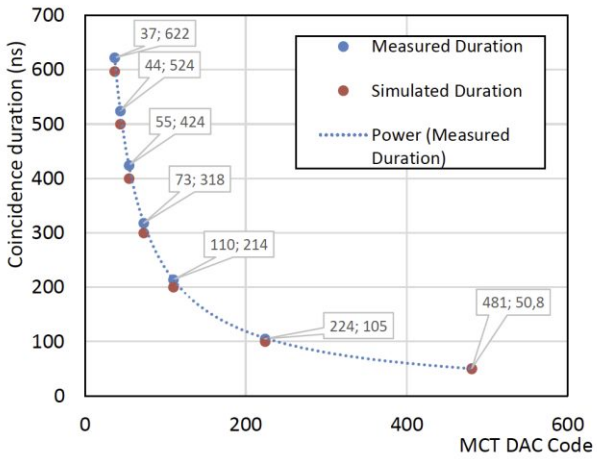

Figure 7: Measurement and simulation of the programmable code and the coincidence time duration.

Each coincidence sub-unit has 68 pairs of configuration registers: V_1 to V_{68} for vetoing and M_1 to M_{68} for masking. V_i = 0 sets input *i* for coincidence, V_i = 1 sets input *i* for anti-coincidence. M_i = 0 disables input *i*, and M_i = 1 enables the input. For the digital pattern L_i the counter increments under the following condition:

$$\prod_{i=1}^{68}[(V_i \oplus L_i) + \bar{M}_i] = \begin{cases} 1, & \text{counter increments.} \\ 0, & \text{counter remains constant.} \end{cases}$$

The $\bar{M}_i$ masks by logic OR (+) the output of the logic XOR ($\oplus$) between the digital pattern L_i and the veto V_i. The L_i is the latched trigger pulse from input *i*, where the trigger is masked by M_i. The logic AND ($\prod$) is the coincidence of all 68 factors, and the counter increments if the results is 1. The trigger pulse pattern is latched to prevent glitches (e.g. from pulse height related time walk) and ensure that all trigger pulses are present for evaluation at the end of the coincidence time. The latch is automatically reset after coincidence evaluation.

2.5 Test and gain calibration unit

The ASIC has a circuit for testing and gain calibration. The circuit allows one to inject a calibrated charge into any channel, to measure the pulse height and to observe the counters. The test and gain calibration circuit is designed to produce a programmable voltage step across a programmable capacitor bank to create a charge, which is injected into one preamplifier input. This procedure allows one to measure the channel gain and study the counting depending on the threshold and the input charge.

2.6 Single event latch-up detection unit

The ASIC has two latch-up detection modules (SEL DM) for latch-up protection and recovery. Each SEL DM has two inputs (SELA and SELB) and one output (LU). The SEL DM is used with an external resistor that conducts the ASIC supply current. The SEL DM compares the voltage across the external resistor with the programmed reference. Any latch-up in the ASIC increases the supply current through the external resistor causing the voltage drop to exceed the programmed reference. The external system can cycle (on/off) the power to the ASIC and recover from latch-up. The reference voltage is programmable by a 5-bit DAC to cover the current in the range from 0 to 500 mA in steps of 16 mA assuming an external resistor of 0.2 Ohm.

2.7 ASIC layout

Figure 8 shows the ASIC floor plan, with pad frame and the signals on the chip. One can see the analogue part (green, yellow, blue) on the left and digital part on the right (orange). The pad frame has a total of 167 signals; the channel analogue inputs are all on one side, and digital inputs/outputs are on the opposite side. Figure 9 shows the photograph of the ASIC with view on the top metal layer. The active area is 15.98 mm × 15.98 mm. The ASIC was designed in 0.35-µm CMOS process and has been manufactured at AMS [9].

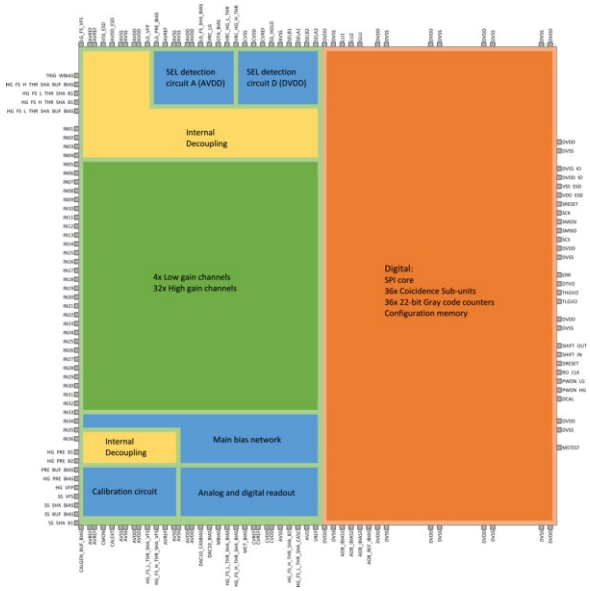

Figure 8: Floor plan with signals and pad frame.

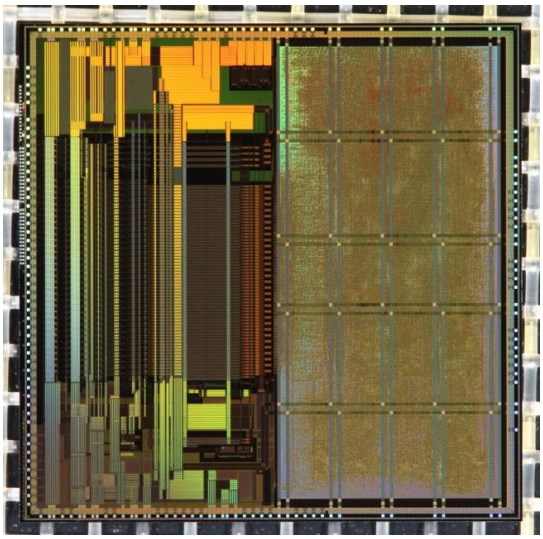

Figure 9: Photograph of the ASIC, view on the top metal layer.

2.8 ASIC test setup for design validation

The ASIC test setup consisted of a National Instruments PXI system (NI PXIe-1082) with a HSDIO (NI PXIe-6544), DAQ (NI PXIe-6363) and FlexRIO (PXIe-7962R, NI-6583) with a NI PXIe-8135 controller running LabView 2015 software. An Applicos PA72G16400 arbitrary waveform generator (AWG) PXI module and external HP33120A AWG were used to generate the input analogue signals. Some measurements used a HP53131A precision counter and Tektronix TDS3014B oscilloscope. Coincidence counter testing used a Berkeley Nucleonics Corporation pulse/delay generator (model: 565) operated in 2-channel mode. The chip under test (device under test, DUT) was mounted in the centre of a custom-made test card (Figure 10).

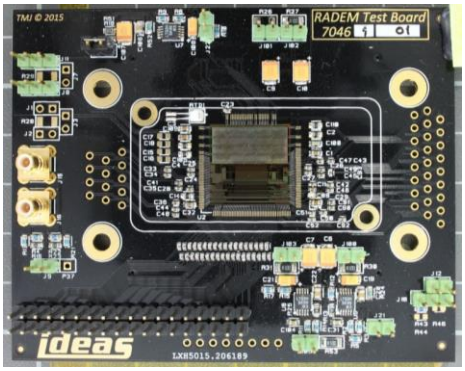

Figure 10: Photograph of the ASIC on a test card, top view.

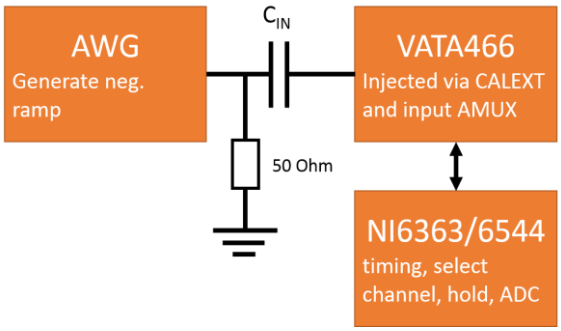

Figure 11: Block diagram of the system used for charge injection in all test cases but for coincidence measurements.

During operation a grounded metal cap covered the ASIC. The test card had low-dropout regulators (LDOs), analogue and digital buffers, and capacitors to the chip analogue inputs. For all analogue input characterisation, the built-in calibration unit (cf. Figure 2) was used with an external high-precision input capacitor connected to pad CALEXT with values of C_{IN} = 10.0 pF +/-1% and 33.0 pF +/-1%. The AC-coupled signal was terminated by 50 Ω close to the inputs. Charge injection Q_{IN} was carried out via a negative ramp waveform with fixed voltage amplitude U_{IN} and frequency f_{IN} following the first-order relation $Q_{IN} = C_{IN} \times U_{IN}$. All measurements were conducted at room temperature (21 °C).

3. PRELIMINARY RESULTS ASIC DESIGN VERIFICATION AND VALIDATION

The following paragraphs summaries the preliminary results for two specific devices under test (DUT1 and DUT2). For the tests we have programmed *DAC_GLOBAL_GAIN* to 864 and 832 for DUT1 and DUT2, respectively, such that the high-gain high threshold (HGHT) range reached 1025 fC. The difference between the devices is expected because of manufacturing process variations. If needed, the DAC parameter could be used to change the threshold range and resolution allowing the ASIC to be used in applications that require different threshold ranges. Both devices were operated at supply voltages of V_{DD} = 3.3 V, V_{REF} = 1.8 V and V_{SS} = 0.0 V, and MBIAS current of 300 µA.

3.1 Slow shaper gain, saturation, non-linearity and noise

Figure 12 shows a measurement with low-gain channel LG04. A 8-pC charge is injected at CALEXT via the 800-mV step across the 10-pF capacitor (green line, labelled 3). The charge exceeds the chosen threshold and triggers a 50-ns wide pulse (red line, labelled 2). The analogue output measured at AVO (yellow line, labelled 1) shows the slow shaper output with 1100-mV amplitude. From the measurement one can calculate the gain of about 1100 mV/8 pC = 137 mV/pC. The fitted LG slope is indeed 0.139 mV/fC (cf. Figure 13). A similar measurement for high-gain (HG) channels gives a gain of 1.36 mV/fC (cf. Figure 13). For both types of channels we measure a slow shaper peaking time τ = 1.3 µs (cf. Figure 12). The trigger pulse width is about 50 ns and has a time walk in the range from a few ns to about 150 ns depending on the threshold and pulse height as expected by the fast shaper rise time. Figure 13 shows the pulse height measured at AVO_BUF versus the charge injected to a high- and low-gain pre-amplifier via CALEXT. The SS_HOLD signal was activated 1.3 µs after charge injection and the held value (pulse height) was measured.

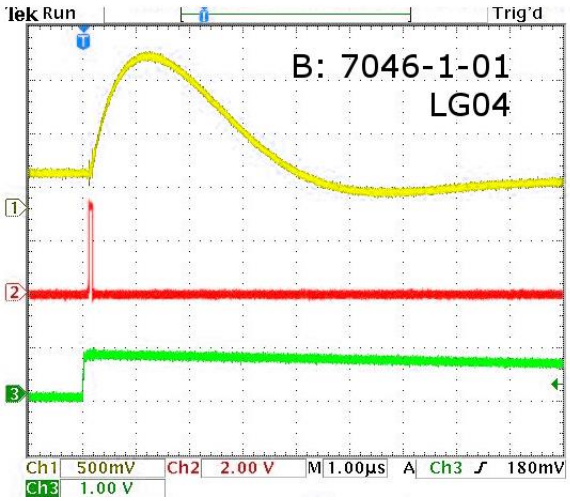

Figure 12: Oscilloscope screenshot with DUT1. The charge of 8 pC was injected into low-gain channel LG04. The yellow line (1, top) shows the slow shaper output, the red line (2, middle) the trigger output and the green line (3, bottom) the input signal.

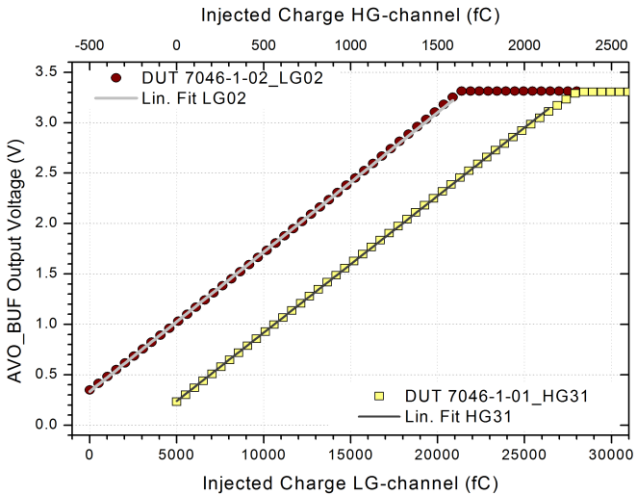

Figure 13: Measurement of the output voltage at AVO_BUF versus injected charge for a high-gain (yellow squares) and a low-gain channel (red circles) with linear fits (lines).

For both types of channels, the pulse height increases linearly with input charge and saturates at about 20.8 pC for low-gain and 2.2 pC for high-gain channels. The offset is slightly different as expected for the shaper output pedestal variations. The statistical error of the measurements is too small to be visible. The integral non-linearity of the analogue output is the maximum absolute deviation between the data and the linear fit to the data.

Figure 14 shows the measurement of the equivalent noise charge (ENC) versus capacitive load at the pre-amplifier inputs in high-gain and low-gain channels. The ENC is input referred noise in units of charge and was measured by the standard deviation of the analogue output signal (AVO) divided by the gain. The ENC increases with capacitive load, as expected, and can be approximated by linear fit for capacitance larger than 100 pF. Table 2 summarises the gain, saturation charge and integral non-linearity measured in high-gain and low-gain channels. These values are representative for the other channels and chips at room temperature.

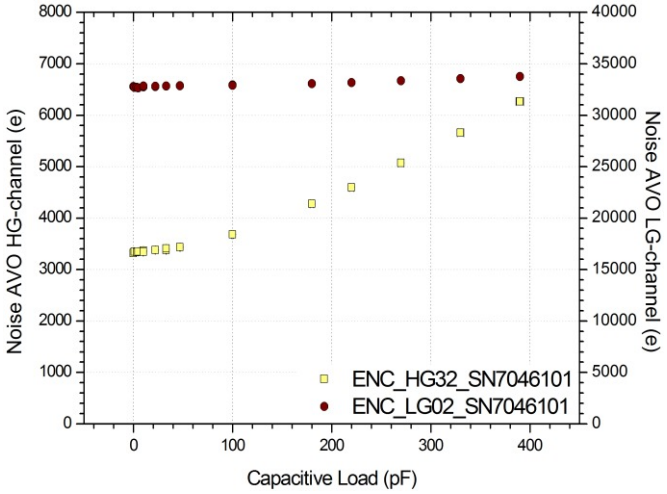

Figure 14: Measurement of the equivalent noise charge versus capacitive load at the pre-amplifier inputs in low-gain (red circles, right y-axis) and high-gain channels (yellow squares, left y-axis).

Parameter		**High-gain channel**	**Low-gain channel**
Gain	[mV/fC]	1.360	0.139
Saturation charge (analogue output)	[pC]	2.2	20.8
Integral non-linearity (analogue output)	[%]	2.5	4.0
ENC	[e]	3320	33000
ENC slope vs. capacitive load	[e/pF]	9	3

Table 2: Summary of the measured gain, saturation charge, integral non-linearity, and equivalent noise charge (ENC).

3.2 Counting threshold range

The accurate calibration of the threshold DACs in units of charge Q is important for the application in RADEM. We have performed this calibration by injecting known charges for several fixed threshold DAC values. For all charges above the threshold, the number of triggers equals to the number of injections, while there are no triggers for charges below the threshold. We define the threshold charge Q_C as the charge for which the normalised counts N, i.e. the ratio of triggers and injections, is $N(Q_C) = 0.5$. Figure 15 shows a measurement of the normalised counts versus input charge for fixed threshold. The data can be approximated by the "error function" $N(Q) = A \times \mathrm{erf}[(Q - Q_C)/w]$ with amplitude A, threshold charge Q_C and width w.

Figure 16, Figure 17, and Figure 18 show the data for a low-gain channel, and the two thresholds in a high-gain channel. The data represents the results for other channels. Table 3 summarises over which range the thresholds can be programmed and the least-significant bit (LSB) step size. The step size is mainly affected by the threshold DAC resolution controlled by the *DAC_GLOBAL_GAIN* parameter, and the noise at the input to the comparator. The results are suitable for the application in RADEM.

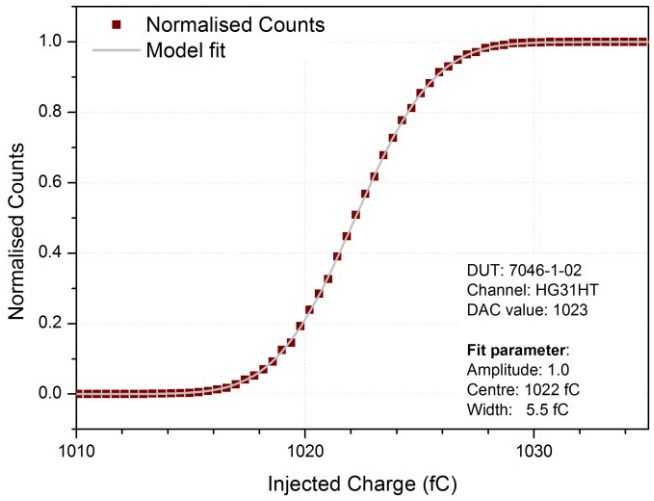

Figure 15: Measurement of normalised counts versus injected charge. The data is fit by an error function.

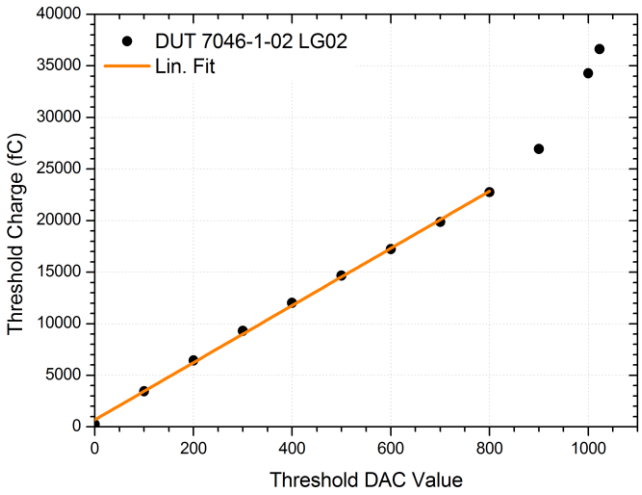

Figure 16: Calibration of the threshold charge over threshold DAC value in a low-gain channel.

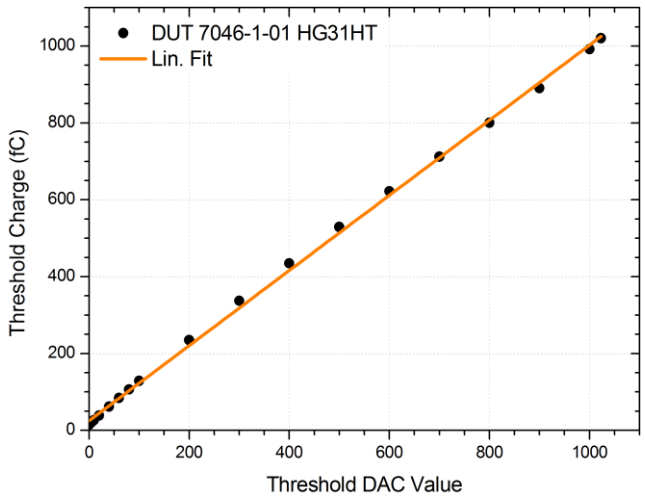

Figure 17: Calibration of the threshold charge over threshold DAC value in a high-gain high-threshold (HGHT) channel.

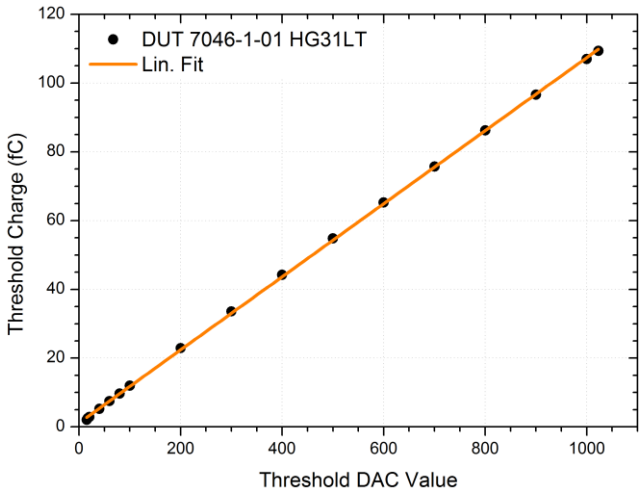

Figure 18: Calibration of the threshold charge over threshold DAC value for a high-gain low-threshold (HGLT) channel.

Table 3: Measurement of the minimum threshold above noise, maximum threshold, and the precision for the three types of thresholds.

	Minimum threshold above noise, measured [fC]	**Maximum threshold, measured [fC]**	**LSB step size [fC]**
Low-gain threshold	260	22800	28
High-gain low threshold	2.2	109	0.1
High-gain high threshold	15	1020	1.0

3.3 Trigger rate capability and input charge rate

RADEM must be able to count at a rate of 100k counts per second (cps) and simultaneously tolerate large input charge rate from the electron background in the radiation sensors. The pre-amplifier gain and feedback resistance are limiting the input charge rate. We measured the trigger rates from a single channel for a given charge rate into a high-gain and low-gain channel. The ASIC internal counters were not used for testing the rate limitation, because they can count at much higher rates than what can be sustained by the pre-amplifiers. We connected the trigger-Or signals TVHGVO or TVLGVO to an external high-precision counter (HP53131A). Only the trigger signal from the chosen channel and comparator was allowed to reach the trigger-OR by masking all other 67 triggers. Figure 19 shows the normalised counts measured versus the input rate with 600 fC in to a high-gain channel and 10 pC into a low-gain channel. The normalised count of 1 indicates that all injected events are counted, while 0 means that none are counted. The measurements show that the high gain channel sustains the input charge rate up to about 3 MHz × 600 fC = 1.8 µA, while the low-gain channel sustains up to at least 100 kHz × 10 pC = 1 µA.

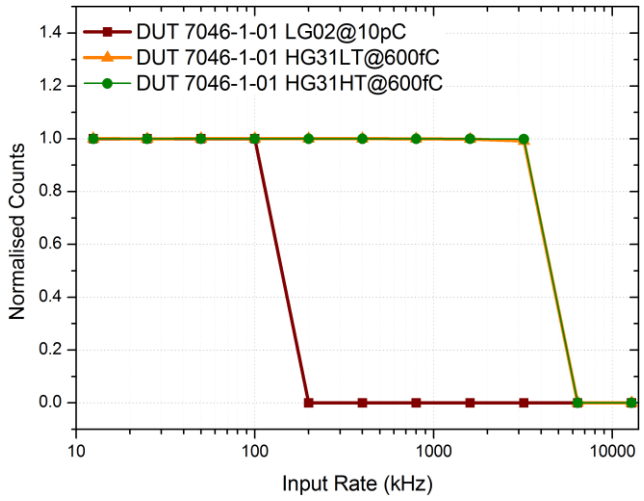

Figure 19: Measurement of the normalised counts versus input rate in a low-gain channel (red), and a high-gain channel (HGLT orange and HGHT green).

3.4 Coincidence counting

In a first test we confirmed that the 22-bit Gray counters increment correctly up to their maximum value and then continue from zero. For the second test we programmed the coincidence unit to trigger on the time coincidence between a high-gain and a low-gain channel (HG06HT and HG32LT) and to count in one of the Gray counters. We programmed the coincidence time of 110 ns. We injected charge pulses at the inputs of channels HG06 and HG32 with a fixed time delay of less than the coincidence time. The time of injecting into HG32 was delayed in a high-precision delay generator. The trigger thresholds were set just above the noise. We acquired the number of counts from the Gray counter register (Counter 1) while charges were injected at 100-kHz frequency into the channels. Figure 20 shows the recorded number of two-channel time coincidences from Counter 1 versus time for the duration of 100 s. One can see that the counter value increases up to 2^{22} = 4194304 and then continues from zero. The count rate can be read off as $2^{22}/40$ s ≈ 100 kHz, which equals the input rate, as expected. Figure 21 shows the counts versus relative trigger delay between the two channels. All coincidences are counted correctly for the relative delay of less than 108 ns and no coincidence are counted for the delay longer than 124 ns, as expected for the coincidence time of 110 ns.

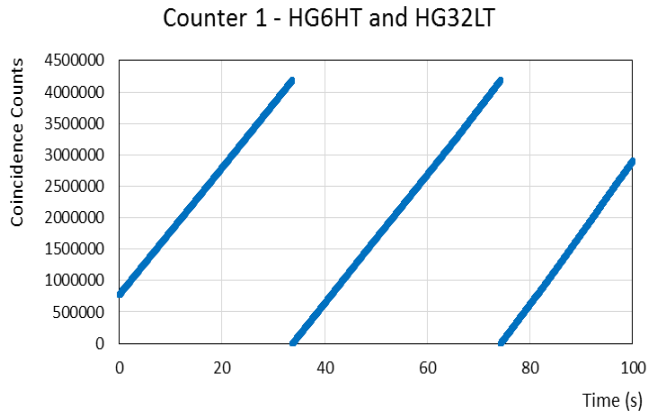

Figure 20: Measurement of the two-channel time coincidences recorded in Counter 1 versus time.

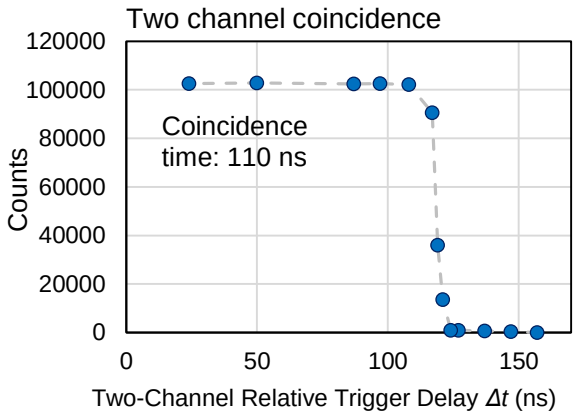

Figure 21: Measurement of the counts versus relative trigger delay between the two channels.

4. CONCLUSION

We have designed the ASIC for the front-end detector readout in the RADEM instrument. A wafer lot has been manufactured and we have tested the design with several chips in the lab. The preliminary results show that the ASIC is fully functional and performs as required for the RADEM instrument. We have implemented similar analogue designs for other space projects and the results are as expected from the previous experience. The digital design of the ASIC with the programmable coincidence pattern unit and Gray counter is entirely new. While the preliminary results of the digital design have not shown any unexpected effects, further tests are needed, i.e., irradiations with heavy ions are planned to test the triple modular redundancy, parity bits and transient filters, and further tests of the coincidence logic are planned with the ASIC assembled in the RADEM engineering model. In general, the combined integration of analogue and digital designs on the same ASIC design allows one to increase functionality and improve the instrument performance in terms of reduced power, smaller volume and lower mass. This is important for RADEM and for the development of future spaceborne systems.

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