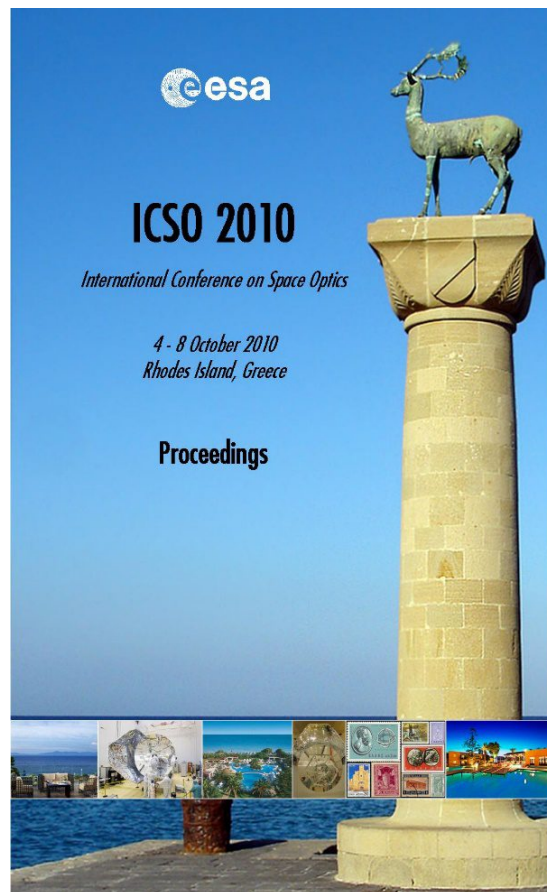# International Conference on Space Optics—ICSO 2010

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SYSTEMS APPROACH TO THE DESIGN OF THE CCD SENSORS AND CAMERA ELECTRONICS FOR THE AIA AND HMI INSTRUMENTS ON SOLAR DYNAMICS OBSERVATORY

N. Waltham[1], S. Beardsley[1], M. Clapp[1], J. Lang[1], P. Jerram[2], P. Pool[2], G. Auker[2], D. Morris[2], D. Duncan[3].
[1]Rutherford Appleton Laboratory, Harwell Business Innovation Campus,
Didcot, Oxon, OX11 0QX. e-mail: nick.waltham@stfc.ac.uk
[2]e2v technologies, 106 Waterhouse Lane, Chelmsford, Essex, UK CM1 2QU.
[3]Lockheed Martin Advanced Technology Center, Dept. ADBS, Bldg. 252, 3251 Hanover St., Palo Alto, CA 94304-1121

ABSTRACT

Solar Dynamics Observatory (SDO) is imaging the Sun in many wavelengths near simultaneously and with a resolution ten times higher than the average high-definition television.

In this paper we describe our innovative systems approach to the design of the CCD cameras for two of SDO's remote sensing instruments, the Atmospheric Imaging Assembly (AIA) and the Helioseismic and Magnetic Imager (HMI). Both instruments share use of a custom-designed 16 million pixel science-grade CCD and common camera readout electronics. A prime requirement was for the CCD to operate with significantly lower drive voltages than before, motivated by our wish to simplify the design of the camera readout electronics. Here, the challenge lies in the design of circuitry to drive the CCD's highly capacitive electrodes and to digitize its analogue video output signal with low noise and to high precision. The challenge is greatly exacerbated when forced to work with only fully space-qualified, radiation-tolerant components. We describe our systems approach to the design of the AIA and HMI CCD and camera electronics, and the engineering solutions that enabled us to comply with both mission and instrument science requirements.

I. INTRODUCTION

The first of NASA's Living with a Star program, Solar Dynamics Observatory (SDO) was launched from Cape Canaveral, Florida, on 11 February 2010 and maneuvered into a geosynchronous sun-pointing orbit that allows near continuous observations of the Sun. Over a nominal five year mission lifetime, extendable to ten years, SDO is enabling scientists to investigate the causes of solar variability, the structure of the Sun's magnetic field and the space weather generated by the solar wind, solar flares and coronal mass ejections from the Sun's atmosphere. Two of SDO's three remote sensing instruments are the Atmospheric Imaging Assembly (AIA) led from the Lockheed Martin Solar and Astrophysics Laboratory in Palo Alto, California, and the Helioseismic and Magnetic Imager (HMI) led from Stanford University. The CCDs were provided by e2v technologies Ltd, Chelmsford, UK, and the CCD camera electronics from the UK's Rutherford Appleton Laboratory (RAL). The overall program was managed by Lockheed Martin.

AIA is studying the evolution of the solar coronal magnetic field, taking images that span 1.3 solar diameters and with a resolution ~ 1 arcsecond. It consists of four telescopes with switchable filters that enable imaging in seven discrete EUV wavebands, each of a well-defined spectral line and indicative plasma temperature. One telescope has filters to observe in three visible/UV wavebands. The four telescopes can be read out together and an entire data set can be acquired with a cadence ~ 10 seconds. HMI is observing the motions of the Sun's surface or photosphere and solar oscillations. It measures the polarization of the full solar disk with a resolution ~ 1 arcsecond and at the discrete visible-light wavelength of 617 nm. The aim is to determine the internal sources and mechanisms of solar variability and how the physical processes inside the Sun relate to the surface magnetic field.

Wishing to minimize design costs, the instrument teams at Lockheed Martin and Stanford University agreed to a common procurement specification for the AIA and HMI CCDs: a 4096 x 4096 pixel science-grade CCD with 12 µm pixel pitch, currently the largest CCD to have ever flown in a space mission. To satisfy the requirement for high cadence, the four 2048 x 2048 pixel quadrants of the CCD would need to be read out concurrently through four corner output amplifiers, each running at 2 Mpixels/s. Front-illuminated sensors were specified for the HMI instrument and back-illuminated EUV-sensitive sensors for the four AIA telescopes. The most challenging requirement however, was for the CCD to run with lower DC bias and drive clock voltages than previous e2v CCDs whilst still retaining nominal pixel full-well capacity, charge-transfer characteristics and output signal linearity. If successful, it would ease the selection of appropriate space-qualified electronic components, enable the design of simpler and more compact readout circuitry, and reduce power dissipation in both the CCD and the electronics. All of these benefits would also increase the reliability of the design. An added bonus would be the CCD's greater immunity to the cumulative effects of ionizing radiation over the long mission lifetime.

II. SYSTEMS APPROACH TO THE CCD AND CAMERA ELECTRONICS DESIGN

Space missions invariably call for the design of extremely light and compact electronics systems of minimal power dissipation, yet they must also survive the vibrations experienced during launch and then the harsh thermal environment and the damaging effects of space radiation. The designer of space electronics therefore faces severe challenges that are compounded by having to work from a relatively small catalogue of high-reliability, space-qualified, radiation-tolerant components that are acceptable and approved for use by international space agencies such as NASA and ESA.

CCDs are analogue devices that require relatively high drive voltages compared to digital components. Their operation relies on the sequenced pulsing or clocking of multi-phase electrodes to shift the signal charge collected within pixels through the substrate and out to one or more charge detection amplifiers. The drive clocks are typically ~ 10 V amplitude and must have sufficient current drive for the CCD's electrode capacitance. A charge detection amplifier requires ~ 30 V of low-noise DC bias and provides a video signal output swing ~ 1 V. Prior to analogue-to-digital conversion, correlated double sampling (CDS) enables the true video signal to be extracted from the output which otherwise contains artifacts from the CCD clocks and reset noise. Analogue-to-digital conversion to 14-bit accuracy was specified for the AIA and HMI cameras.

Lockheed Martin invited RAL to design, manufacture and qualify the CCD camera electronics for AIA and HMI; RAL having previously developed the cameras for the remote sensing imagers now flying on NASA's Solar Terrestrial Relations Observatory (STEREO), a pair of solar observatories launched in October 2006 [1,2]. The CCD for the STEREO mission was an off-the-shelf device requiring the electronics to be designed around a given specification. In contrast, the CCD for AIA and HMI was to be a custom-design and so e2v technologies and RAL were afforded the opportunity of taking a systems approach to the design of both the CCD and camera electronics. There were three key issues that we wished to address:

A. CCD Serial Register Drive Clock Amplitude

The instrument science requirements called for the CCD to be read in a split-frame readout mode through four corner output amplifiers, each running at 2 Mpixels/s and thus enabling the CCD's 16-million pixels to be read in just over 2 seconds. Readout through just two output amplifiers; left-hand, right-hand, top or bottom pairs was also specified to provide a degree of redundancy in the event of a readout channel failure. This degree of flexibility demanded independent drive of 10 serial register electrode phases, 5 for each of the top and bottom registers. The design of our 10 V amplitude serial register clock buffer for the STEREO cameras was based on a circuit topology of discrete bipolar transistors with associated diodes, resistors and decoupling components. Implementation of 10 channels for the SDO camera would require significant printed circuit board (PCB) real-estate. We recognized that if we could reduce the drive clock amplitude to just 5 V without compromising the nominal serial register well capacity and/or charge-transfer characteristics then we could replace all the discrete circuitry with a single space-qualified 16-channel CMOS logic buffer IC. We would have an almost ten-fold reduction in PCB real-estate requirement, a significant reduction in power dissipation in both the CCD and the camera electronics, and a very much more reliable design due to the large reduction in component count.

B. CCD Video Output Amplifier Bias

We also identified a significant saving in circuit complexity, component count and power dissipation to be gained from operating the CCD's output amplifier bias at ≤ 26 V compared to the ~ 30 V bias of previous CCDs. Our cameras employ a compact off-the-shelf, space-qualified, triple-rail DC-DC converter module configured to provide + 5 V, + 15 V and + 30 V secondary rails from a 28 V primary bus input. Space-qualified operational amplifiers (op-amps) are used to generate the CCD's low-noise DC bias supplies. We add a pulse-width-modulation (PWM) converter to create a 36 V rail from the 30 V supply, enabling a 30 V bias to be generated from the 36 V rail whilst still allowing margin on the available voltage swing. However, the maximum operating supply of our selected space-qualified op-amp is 30 V and we have yet to identify a suitable alternative that will operate from 36 V. We have to add a bipolar transistor emitter-follower within the feedback loop of the op-amp with the op-amp supplied from the 30 V rail and the transistor from the 36 V rail. Although this circuit operates satisfactorily, it is not an elegant design. We recognized that if we could operate the CCD's output amplifiers with ≤ 26 V bias, we could dispense with the PWM converter and operate the op-amps direct from the DC-DC converter's 30 V rail and dispense with the transistor buffers.

C. Dummy Video Output Amplifiers

We also wanted to address the problem of conveying the CCD's low-level analogue video signals from the focal plane assembly to the camera electronics without incurring extraneous noise pickup. This usually requires

very careful design of the interconnecting harness and rigorous attention to the overall electrical grounding of the CCD-electronics system. We specified that each of the CCD's output amplifiers should be provided with an additional 'dummy' amplifier that would receive no signal charge but in all other respects present an output of near identical electrical characteristics to the real output amplifier. Passing both signals to the camera electronics and subtracting them would enable a high degree of common-mode rejection of noise induced in the harness and a first-order rejection of electronic and/or thermal drifts in the output amplifier. The disadvantage of the dummy is a $\sqrt{2}$ increase in the total CCD readout noise over a 'perfect' single-ended output. However, we fully anticipated that this extra noise would be more than compensated for by the better common-mode rejection of the other system noise components.

III. LOW-VOLTAGE CCD

e2v technologies established a manufacturing process using a reduced dielectric thickness between the CCD electrodes and the underlying silicon such that the same charge storage density as standard devices could be obtained with 7 V imaging area clock voltages. Modeling showed that we would achieve the required 150k to 200k electrons full-well capacity within a 4-phase 12 µm pixel. Operation with 5 V clocks reduces the charge storage density. For the serial register, we therefore increased the width and hence the charge storage area of the pixels to recover > 200k electrons charge handling capacity. The thinned dielectric process also reduces transistor bias requirements, allowing output amplifier operation with ~ 22 V bias.

Thinning the dielectric of a 50 x 50 mm CCD carried the risk of an increase in the number of shorts to substrate. Such shorts are fatal and so could reduce manufacturing yield sufficiently to threaten the viability of a flight program. A proof-of-concept development program was therefore initiated, from which first results were extremely encouraging with all basic imaging and charge storage characteristics appearing to have been met. However, more exhaustive testing revealed a low-level smearing of charge in the imaging area columns with strong evidence of charge ~ 100 electrons being deferred at the imaging area to serial output register boundary. It was also found that the problem could be largely eliminated by running the serial register clocks with 6 V amplitude. A subsequent modification in mask design and a second generation of devices enabled fully satisfactory operation with 5 V clocks. However, by this point in the program we had already identified a space-qualified, radiation-hard CMOS buffer compliant with nominal operation at 6 V and an absolute maximum rating of 7 V. The use of this IC, operated at 6 V, would provide increased operating margin and enabled us to retire all risk concerning the initial deferred charge issue of early devices.

IV. CAMERA READOUT ELECTRONICS

Each AIA and HMI CCD (Fig 1) is driven and read out through its own dedicated Camera Electronics Box (CEB). It has dimensions of 152 mm x 131 mm x 95 mm and a mass of 2.9 kg. The enclosure walls are 5 mm thick aluminum to ensure sufficient attenuation of space radiation over mission life. During exposures the CCD and CEB consumes 12 W rising to 17 W during readout. The CEB contains four electronics cards mounted above a separately screened input filter and DC-DC power converter. A photo of the assembled unit, minus front panel and lid, is reproduced in Fig 2. The upper-most card carries four video processing and digitization ASICs operating in parallel at 2 Mpixels/s and each connected to one of the CCD's quadrant readout amplifiers. The second card in the stack provides all of the CCD's low-noise DC bias voltages. Supplies to each of the CCD's output amplifiers are buffered separately to minimize crosstalk between channels. An 8-channel 10-bit DAC ASIC enables software programming and fine adjustment of the bias supplies. Telemetry circuitry internal to the CEB allows monitoring of the CEB's secondary power rails, CCD bias voltages and the CCD and CEB operating temperatures. The third card carries a waveform generator and sequencer ASIC and sufficient clock driver buffers to enable CCD readout through any or all of its quadrant readout amplifiers. The final card provides a SpaceWire communications interface with the main AIA or HMI control electronics. A single link is used for programming the CEB's ASICs and registers, commanding a CCD readout and the return of the CCD's digitized video data at 200 Mbits/s.

A key component of the camera electronics is a custom-designed and space-qualified CCD video signal processing and digitization ASIC [3,4]. It provides 2 Mpixels/s video amplification, CDS processing and 16 bit digitization of a 1 V input signal. The design is fully-differential to aid rejection of common-mode noise. A 10-bit DAC enables ± 500 mV of programmable DC offset to be introduced into the video signal and a 7-bit programmable x1-x3 gain amplifier enables the ADC to be matched to the required CCD signal swing. The ADC is a 16 bit fully-differential pipelined converter using feedback capacitor switching in the amplifier stages, and over-ranging at intervals in order to minimize differential non-linearity due to capacitor mismatching and amplifier gain errors. Triple-voting logic is used to enhance the single-event upset tolerance of the logic and registers. The ASIC was manufactured on a 0.35 µm 3.3 V CMOS process known for its excellent tolerance to ionizing radiation. With its inputs grounded, the ASIC's noise is 3.5 ADU rms in 16 bits or 53 µV rms. The

CCD provides ~ 4.5 μV/ e⁻ and so the equivalent noise is ~ 12 e⁻ rms. The combined noise floor of the CCD and electronics is ~ 4 ADU rms or ~ 16 e⁻ rms. The power consumption from a 3.3 V supply is 400 mW.

Six flight unit CEBs were manufactured and qualified for AIA and HMI together with two flight-spare units. All units underwent rigorous vibration and thermal cycling environmental qualification prior to delivery.

V. SDO IMAGERY

SDO is returning imagery of phenomenal resolution (Fig 3), providing new insight into the evolution of our Sun's volatile magnetic fields and promises to open up many new avenues of research as the mission develops.
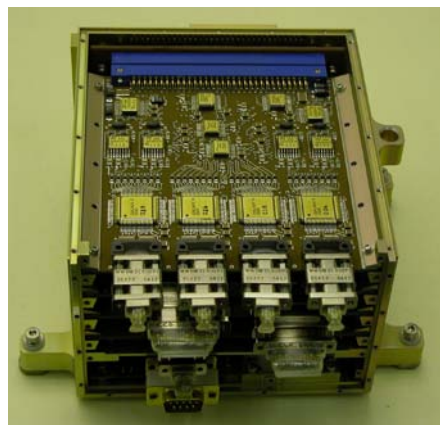

Fig 1. e2v technologies SDO CCD
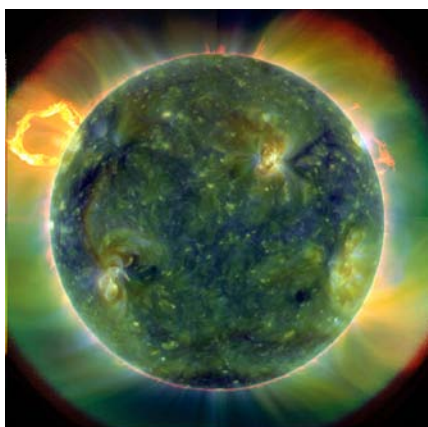

Fig 2. SDO Camera Electronics Box

Fig 3. AIA Imagery: Left: a composite of three wavelength bands, corresponding to temperatures from 700,000 to 2,000,000 Kelvin (hotter = red, cooler = blue). Right: prominence eruption from 30 March 2010 imaged at 304 Å to reveal He II corresponding to a temperature of ~ 50,000 Kelvin. © NASA.

ACKNOWLEDGEMENTS

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