Metrology (including Materials Characterization) for Nanoelectronics

A.C. Diebold, J. Price, and P.Y. Hung
SEMATECH, 2706 Montopolis Drive, Austin, TX 78741

ABSTRACT

Integrated circuits have already entered the world of nanoelectronics. According to the International Technology Roadmap for Semiconductors, the industry will be extending CMOS technology through new materials and device structures for at least the next fifteen years. During that time, the gate length of nanotransistors will shrink to less than 10 nm. The electrical properties of nano-transistors will move into regime of short channel devices where new physics will result in changes in transistor operation. The number of transistors in a single IC is already approaching a number that results 2 billion functions per IC by 2010. Nano-sized features and high density will challenge metrology and characterization and most certainly move measurement further into the world of nanotechnology. Beyond CMOS, new nano-technology based devices are being considered as a means of continuing the rapid pace of technological innovation in electronics.

1. INTRODUCTION

Since the metrology needs for nanoelectronics were recently reviewed[1], this paper will discuss the impact of nano-sized features on measurement. In order to facilitate this discussion, the evolution of transistors is first described.

Transistor Evolution

The transistors found in leading edge microprocessors have characteristics that are different from their microelectronic counterparts of five years ago. Saturation drive current is a key example of a transistor property that is no longer determined by the same properties as long channel transistors [2]. The importance of saturation drive current can be illustrated by considering a simple inverter circuit as shown in Figure 1. The transistor delay (switching speed) τ in an inverter is inversely proportional to the saturation drive current I_{dsat} as described in Equation 1 where (C_{load} is the capacitive load which is approximately equal to the capacitive load of the inverter to ground plus the capacitive load to the line that carries V_{dd}) [3]:

$$\tau = C_{load}\, V_{dd}/I_{dsat} \qquad \textbf{Eq. [1]}$$

In long channel devices, I_{dsat} is inversely proportional to gate length and the EOT under inversion conditions. It is directly proportional to the carrier mobility.

Long channel transistors

$$I_{dsat} = (W/L)\, \mu eff\, Cox\, [0.5\, V_{dsat2}] \qquad \textbf{Eq. [2]}$$

Transistor properties are transitioning to those of short channel devices over the next 15 years. Short channel devices show an increase I_{dsat} when mobility is improved. For very short channel devices, the gate length and carrier mobility do not appear in the approximate expression for drive current I_d. Approximate expressions for I_{dsat} are [3, 4, 5, 6]

Very short channel devices

$$I_{dsat} \sim W\, Cox\, (V_g - V_t)\, \nu_{sat} \qquad \textbf{Eq. [3]}$$

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Here, μ_{eff} is the carrier mobility, W is the transistor width. $V_{dsat} = (V_g - V_t)$, and C_{ox} is the capacitance of the gate dielectric (reduces as gate length shrinks), and V_g and V_t are the gate and threshold voltages respectively. In Eq. [3], L is the electrical (effective) gate length. [4, 5] v_{sat} is the carrier saturation velocity. Lundstrom[5] and Natori[6] have shown that I_{dsat} is limited by how many carriers pass over the barrier at the source of a short channel transistor. Once the carriers overcome the barrier, they move quickly through the channel to the drain. The carrier velocity is dependent on the mobility at the barrier.[5, 6] As stated above, the gate length and carrier mobility no longer directly appear in the functional dependence of $I_{dsat.}$

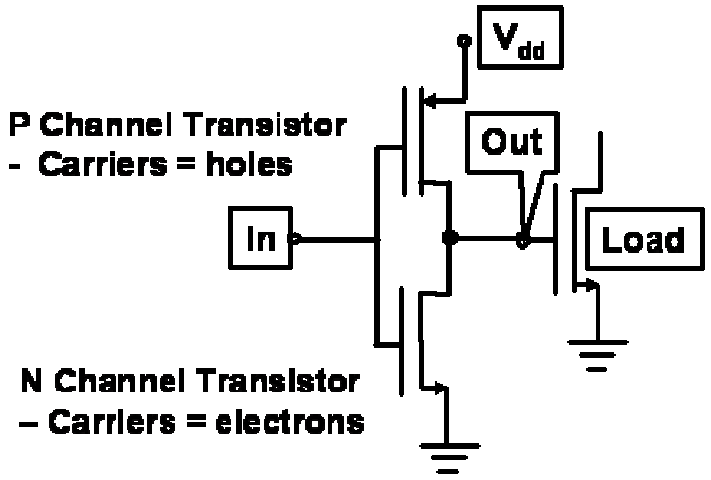

Figure 1. Simple Inverter Circuit showing a transistor load on the out line.

Metrology Needs Based On Transistor Evolution

Both the nano-size induced electrical properties and new transistor designs are driving a number of the future metrology needs of the industry. For example, FINFETs have the transistor channels on the sidewalls of the FINs. Sidewall measurements continue to be very difficult. For example, traditional thin film measurements are done on horizontal layers. FIN thickness is a new Critical Dimension. The need for traditional CD measurements for any nanotransistor is not immediately clear based on the change in functional dependence of the saturation drive current.

Because the saturation drive current of sub 10 nm transistors is not a function of gate length, one might hope that the allowable range of CD values will increase for short channel devices. However, Likharov has shown using a dual gate transistor model that transistor characteristics such as threshold voltage become more sensitive to gate length variation when CD decreases from 10 nm to 5 nm.[7] A dual gate transistor with a 5 nm gate length, 2 nm channel thickness and gate dielectric thickness of 1.5 nm requires CD control to be ~ 0.2 nm with a measurement precision of ~ 1/10 this value.[7]

A number of the measurement need for future transistors involve materials or structures are impacted by nano-scale properties such as quantum confinement. Specifically, dimensionally confined semiconductor structures such as very thin silicon or germanium layers on SOI substrates and single crystal FINs should have their properties impacted by Quantum Confinement.

Nanotechnology Aspects of Metrology for Future Technology

The ITRS roadmap shows that very thin silicon (that is fully depleted of carriers) on insulator (FD-SOI), strained silicon on insulator (sSOI), strained silicon on silicon germanium, and germanium channels are under considered a means of extending CMOS to future technology generations. Spectroscopic ellipsometry is used to measure the top silicon and insulator film thickness. As previously reported, the optical model for the dielectric function of very thin

top silicon layers will be different from the bulk based on quantum confinement and surface states as well as lattice strain.[8].

The optical response of crystalline semiconductors is characterized by critical points where electrons are excited from the top of a valence band to the conduction band minima. This is true for both direct and indirect band gap semiconductors. The critical points are defined as constant energy separation regions of **k**-space that result in a large gradient in the joint density of states where the probability of light absorption is high. In silicon, the E_o' (~3.32 eV) and E_1 (~3.38 eV) critical points are nearly degenerate, with E_o' being represented by a 2D critical point line shape corresponding to the maxima in the real part of the dielectric function, and the E_1 transition represented as an excitonic line shape corresponding to the dominant shoulder in the imaginary part of the dielectric function. For perturbations in the dielectric function such as strain or quantum confinement, it is the E_1 critical point that is most affected. Other critical points in silicon include the feature seen in the optical spectrum at ~4.25 eV (~292nm) called the E_2 critical point.[9]

A recent study has demonstrated the error associated with use of bulk silicon optical constants for ellipsometric measurement of very thin SOI.[8] A nearly 20 % difference between TEM and ellipsometry is observed for sub 2 nm SOI.[8] In Figure 2, we show the change in the imaginary part of the dielectric function vs silicon thickness for very thin SOI. One important feature of the dielectric function is the shift in the energy of the E1 critical point with silicon thickness. The critical point energies were extracted from the ellipsometric data after fixing the film thickness using TEM data.[8] The measurement of unknown semiconductor film thickness can be done using the measured critical point energies.[8]

In a similar fashion, the dielectric function of FINFET FINs should be different from that of bulk crystalline silicon. Recent theoretical studies of nanowires serve as a hint into the extent of these changes.[10] A strong optical anisotropy in silicon nanowires less than 2.2 nm in diameter and the appearance of new low energy absorption peaks for light polarizations along the wire axis.

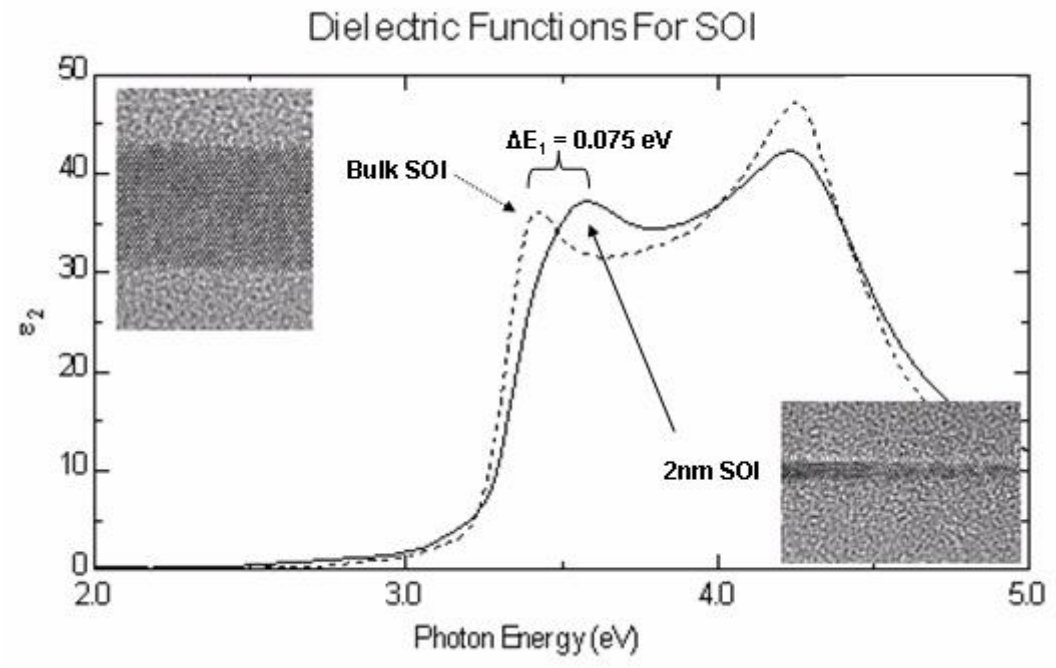

Figure 2. The shift in the E1 critical point of silicon is shown for a 2 nm thick SOI film.

MATERIALS CHARACTERIZATION

TEM imaging and electron diffraction of nanowires has proved a preview of the challenges associated with nano-sized transistor features. TEM images and diffraction patterns often require interpretation of the image using simulations. The appearance of twinning structures in nanowires is one example. Another is the appearance of forbidden spots in TEM diffraction patterns.

The latest generation of commercially available TEM systems are equipped with aberration corrected lens technology which greatly improves imaging. Sub 0.1 nm resolution has been achieved in the high resolution TEM mode, enabling near atomic imaging. Silicon nanowires fabricated using the supercritical fluid-liquid-solid approach have been used to evaluate nanowire imaging and electron diffraction[11]. In Figure 3, we show an image of a silicon nanowire with a <112> growth direction. It exhibits multiple twins running the length of the wire. Gold nanocrystals serve as crystallization seeds for the Si nanowires. The higher resolution image exhibits what appears to be epitaxial interfacing between the two materials. The many twins observed in this image indicate that the nanowire does not have perfect crystal structure. However, image interpretation requires simulation.

A complete interpretation of TEM images involves understanding of interaction of electrons with the atoms in the crystal lattice. The finite size of the nanowire requires a simulation tool that does not rely on the typical periodic boundary conditions that can be employed in extended solids and thin films. Our simulations show that a single twin running down a nanowire can appear as multiple twins, depending on the observation angle.

Electron diffraction of nanowires exhibit previously un-explored phenomena such as forbidden diffraction spots.[12] Simulating the nanowire diffraction patterns is one means of understanding the origin of the additional spots. Although the extra diffraction spots are due to the lack of a bulk lattice structure, the exact pattern seems to reflect both the nanowire size and the facet surface morphology.

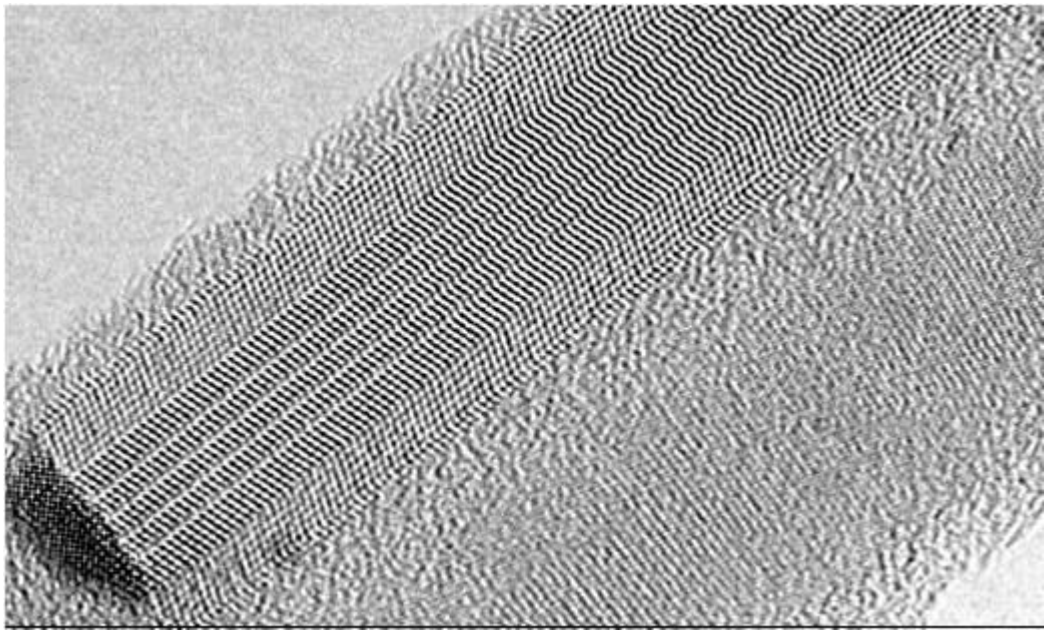

Figure 3. Silicon Nanowire grown for Korgel Group and imaged by Alex Thesen. Figure courtesy Alex Thesen of Zeiss.

CONCLUSION

In this paper, a previous review of metrology needs for nano-electronics was expanded to include the impact of nano-size on materials properties and measurement. Although nano-size is frequently considered to increase difficulty, this paper has illustrated some areas where new materials properties may make measurement easier. The need for simulation of TEM images of nano-sized materials was also described.

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